

Datasheet

APM32E103xCxE

Arm® Cortex®-M3 based 32-bit MCU

Version: V1.8

1. Product characteristics

■ Core

- 32-bit Arm® Cortex®-M3 core
- Up to 120MHz working frequency

■ On-chip memory

- Flash: 512KB
- SRAM: 128KB
- EMMC: Supports CF card, SRAM, PSRAM, SDRAM NOR and NAND memory

■ Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

■ Reset and power management

- V_{DD} range: 2.0~3.6V
- V_{DDA} range: 2.0~3.6V
- V_{BAT} range of backup domain power supply: 1.8V~3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported(PVD)

■ Low-power mode

- Sleep, stop and standby modes supported

■ DMA

- Two DMA; DMA1 supports 7 channels and DMA2 supports 5 channels

■ Debugging interface

- JTAG
- SWD

■ I/O

- Up to 112 I/Os
- All I/Os can be mapped to external interrupt vector

- Up to 87 FT input I/Os

■ Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 3 USART, 2 UART, support ISO7816, LIN and IrDA functions
- 3 SPI (18Mbps) interfaces, two of which support I2S interface multiplexing
- 2 CAN, USBD and CAN can work independently at the same time

- 1 USBD

- 1 SDIO Interface

■ Analog peripherals

- 3 12-bit ADCs
- 2 12-bit DACs

■ Timer

- 2 16-bit advanced timers TMR1/8 that can provide 7 channels PWM output, support dead zone generation and braking input functions
- 4 16-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 16-bit basic timers TMR6/7
- 2 watchdog timers: one independent watchdog IWDG and one window watchdog WWDG
- 1 24-bit autodecrement SysTick Timer

■ RTC

- Support calendar and clock functions

■ 84Bytes backup register

■ FPU

■ CRC computing unit

■ 96-bit unique device ID

■ Chip packaging

- QFN48/LQFP48/LQFP64/LQFP100/LQFP144

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2. Product information

See the following table for APM32E103xCxE product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32E103xCxE Series Chips

Product		APM32E103xCxE									
Model		CC	CE	CC	CE	RC	RE	VC	VE	ZC	ZE
Package		QFN48		LQFP48		LQFP64		LQFP100		LQFP144	
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@120MHz									
Operating voltage		2.0~3.6V									
Flash(KB)		256	512	256	512	256	512	256	512	256	512
SRAM(KB)		64	128	64	128	64	128	64	128	64	128
EMMC		0						1（Not supported SDRAM）		1（support SDRAM）	
GPIOs		37				51		80		112	
Communi cation interface	USART/UART	3				3/2					
	SPI/I2S	3/2									
	I2C	2									
	I2C3	1									
	USBD	1									
	CAN	2									
	SDIO	0				1					
Timer	16-bit advanced	1				2					
	16-bit general	4									
	16-bit basic	2									
	System tick timer	1									
	Watchdog	2									
Real-time clock		1									
12-bit ADC	Unit	2				3					
	Channel	10				16				21	
12-bit DAC	Unit	2									
	Channel	2									
Operating temperature		Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ Junction temperature: -40℃ to 105℃/-40℃ to 125℃									

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32E103xCxE Series LQFP144 Pins

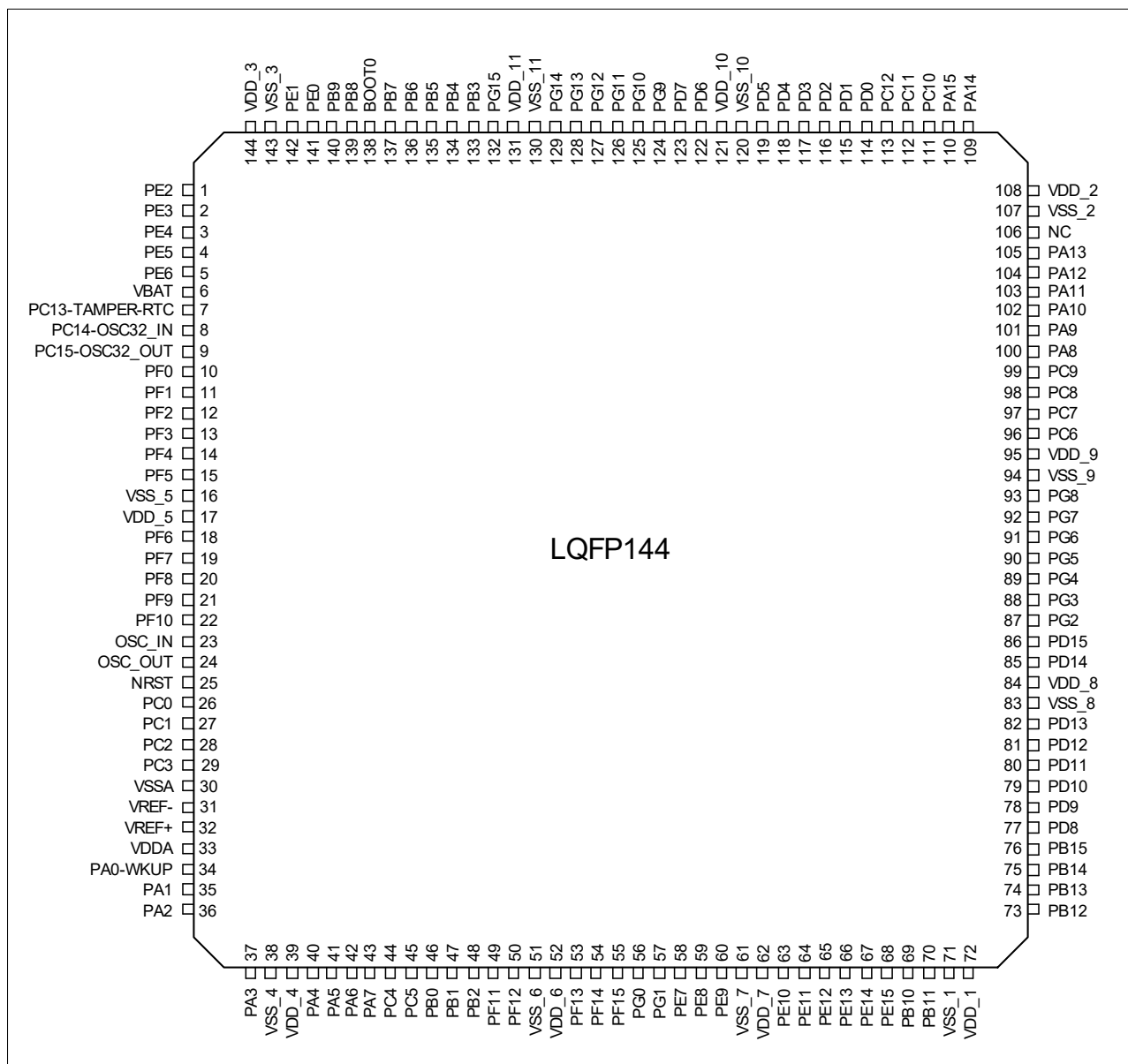


Figure 2 Distribution Diagram of APM32E103xCxE Series LQFP100 Pins

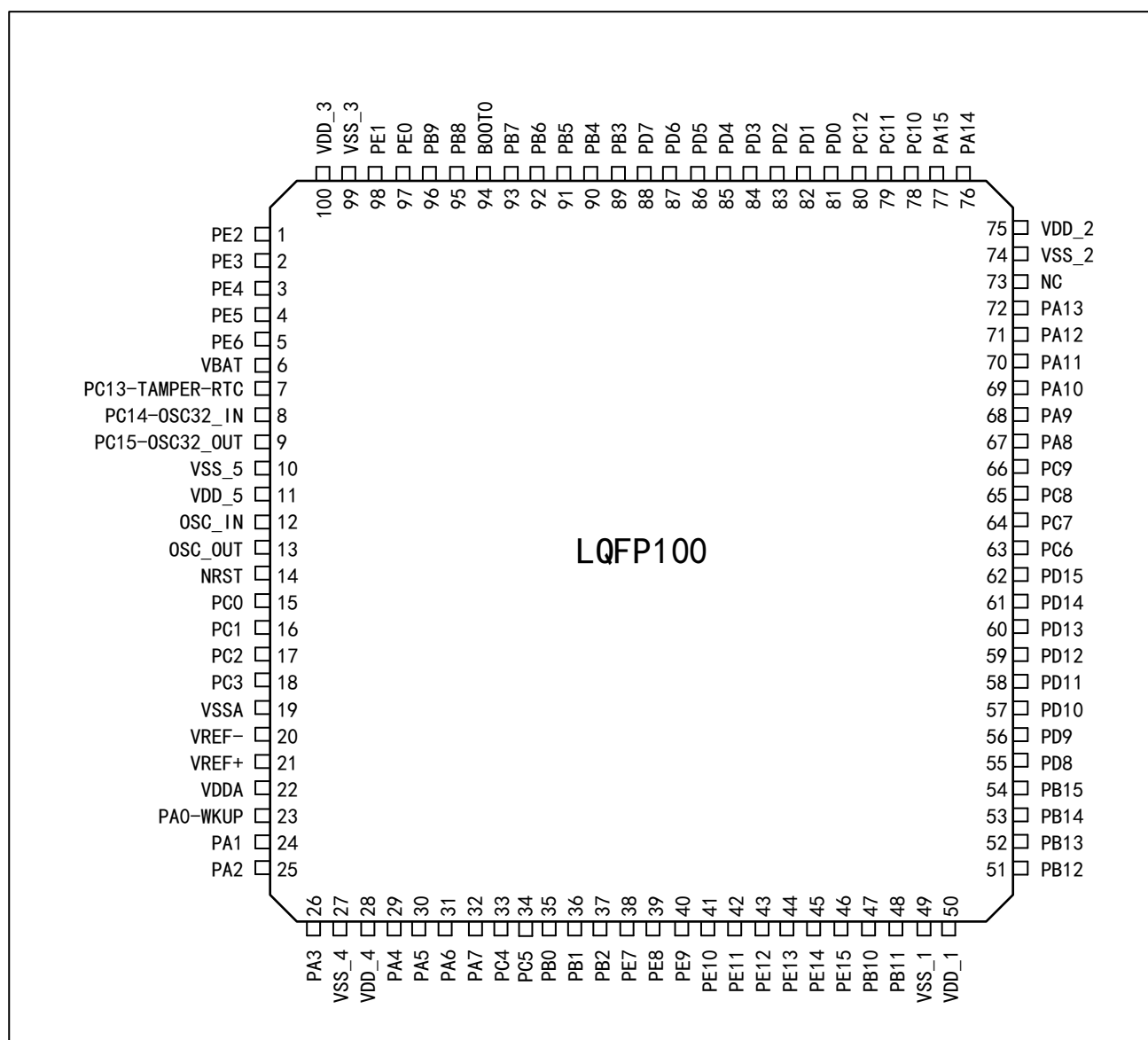


Figure 3 Distribution Diagram of APM32E103xCxE Series LQFP64 Pins

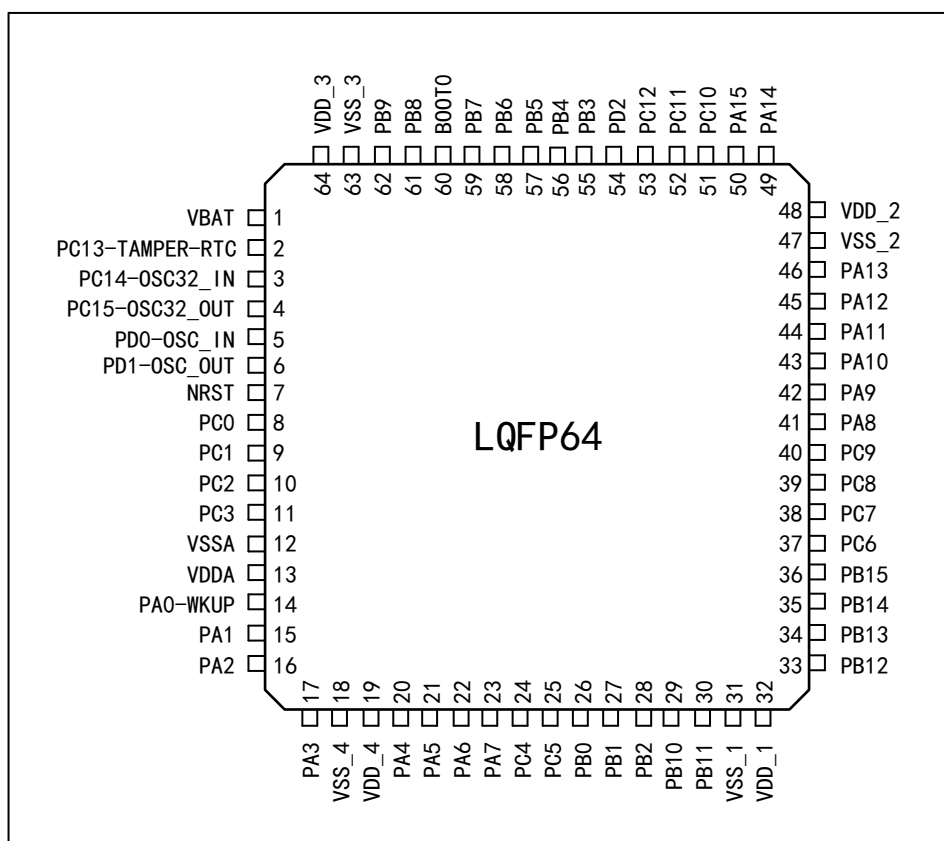


Figure 4 Distribution Diagram of APM32E103xCxE Series LQFP48 Pins

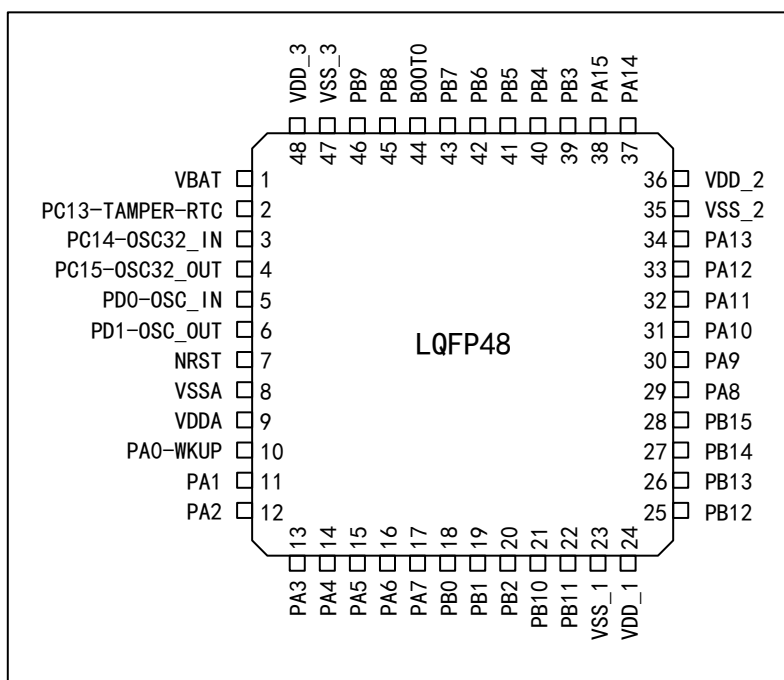
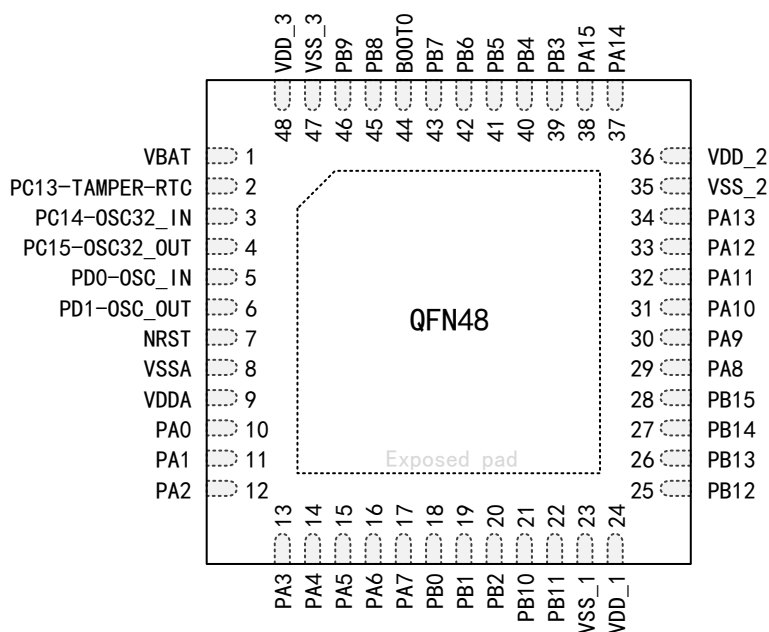


图 5 Distribution Diagram of APM32E103xCxE Series QFN48 Pins



3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM+ function
	STDA	I/O with 3.3 V standard, directly connected to ADC
	STD	I/O with 3.3 V standard
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor
Note	Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register
	Remap	Select this function through AFIO remapping register

Table 3 Description of APM32E103xCxE by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
PE2	I/O	5T	TRACECK, SMC_A23	-	-	-	1	1
PE3	I/O	5T	TRACED0, SMC_A19, DMC_DQ4	-	-	-	2	2
PE4	I/O	5T	TRACED1, SMC_A20	-	-	-	3	3
PE5	I/O	5T	TRACED2, SMC_A21, DMC_DQ5	-	-	-	4	4
PE6	I/O	5T	TRACED3, SMC_A22, DMC_DQ6	-	-	-	5	5
V _{BAT}	P	-	-	-	1	1	6	6
PC13-TAMPER- RTC (PC13)	I/O	STD	TAMPER_RTC	-	2	2	7	7
PC14- OSC32_IN (PC14)	I/O	STD	OSC32_IN	-	3	3	8	8
PC15- OSC32_OUT (PC15)	I/O	STD	OSC32_OUT	-	4	4	9	9
PF0	I/O	5T	SMC_A0, DMC_DQ7	-	-	-	-	10
PF1	I/O	5T	SMC_A1	-	-	-	-	11
PF2	I/O	5T	SMC_A2, DMC_CS	-	-	-	-	12
PF3	I/O	5T	SMC_A3	-	-	-	-	13
PF4	I/O	5T	SMC_A4, DMC_RAS	-	-	-	-	14
PF5	I/O	5T	SMC_A5, DMC_CAS	-	-	-	-	15
V _{SS_5}	P	-	-	-	-	-	10	16
V _{DD_5}	P	-	-	-	-	-	11	17
PF6	I/O	-	ADC3_IN4, SMC_NIORD, DMC_WE	-	-	-	-	18

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
PF7	I/O	-	ADC3_IN5, SMC_NREG	-	-	-	-	19
PF8	I/O	-	ADC3_IN6, SMC_NIOWR	-	-	-	-	20
PF9	I/O	-	ADC3_IN7, SMC_CD	-	-	-	-	21
PF10	I/O	-	ADC3_IN8, SMC_INTR, DMC_LDQM	-	-	-	-	22
OSC_IN	I	STD	-	PD0	5	5	12	23
OSC_OUT	O	STD	-	PD1	6	6	13	24
NRST	I/O	RST	-	-	7	7	14	25
PC0	I/O	STDA	ADC123_IN10	-	-	8	15	26
PC1	I/O	STDA	ADC123_IN11	-	-	9	16	27
PC2	I/O	STDA	ADC123_IN12	-	-	10	17	28
PC3	I/O	STDA	ADC123_IN13	-	-	11	18	29
V _{SSA}	P	-	-	-	8	12	19	30
V _{REF-}	P	-	-	-	-	-	20	31
V _{REF+}	P	-	-	-	-	-	21	32
V _{DDA}	P	-	-	-	9	13	22	33
PA0-WKUP (PA0)	I/O	STDA	WKUP, USART2_CTS, ADC123_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR	-	10	14	23	34
PA1	I/O	STDA	USART2_RTS, ADC123_IN1, TMR5_CH2, TMR2_CH2	-	11	15	24	35
PA2	I/O	STDA	USART2_TX, TMR5_CH3, ADC123_IN2, TMR2_CH3	-	12	16	25	36
PA3	I/O	STDA	USART2_RX, TMR5_CH4, ADC123_IN3,	-	13	17	26	37

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
			TMR2_CH4					
V _{SS_4}	P	-	-	-	-	18	27	38
V _{DD_4}	P	-	-	-	-	19	28	39
PA4	I/O	STDA	SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4	-	14	20	29	40
PA5	I/O	STDA	SPI1_SCK, DAC_OUT2, ADC12_IN5	-	15	21	30	41
PA6	I/O	STDA	SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1	TMR1_BKIN	16	22	31	42
PA7	I/O	STDA	SPI1_MOSI, TMR8_CH1N, ADC12_IN7, TMR3_CH2	TMR1_CH1N	17	23	32	43
PC4	I/O	STDA	ADC12_IN14	-	-	24	33	44
PC5	I/O	STDA	ADC12_IN15	-	-	25	34	45
PB0	I/O	STDA	ADC12_IN8, TMR3_CH3, TMR8_CH2N	TMR1_CH2N	18	26	35	46
PB1	I/O	STDA	ADC12_IN9, TMR3_CH4, TMR8_CH3N	TMR1_CH3N	19	27	36	47
PB2 (PB2,BOOT1)	I/O	5T	-	-	20	28	37	48
PF11	I/O	5T	SMC_NIOS16, DMC_BA	-	-	-	-	49
PF12	I/O	5T	SMC_A6, DMC_A10	-	-	-	-	50
V _{SS_6}	P	-	-	-	-	-	-	51
V _{DD_6}	P	-	-	-	-	-	-	52
PF13	I/O	5T	SMC_A7, DMC_A0	-	-	-	-	53
PF14	I/O	5T	SMC_A8, DMC_A1	-	-	-	-	54

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
PF15	I/O	5T	SMC_A9, DMC_A2	-	-	-	-	55
PG0	I/O	5T	SMC_A10, DMC_A3	-	-	-	-	56
PG1	I/O	5T	SMC_A11	-	-	-	-	57
PE7	I/O	5T	SMC_D4	TMR1_ETR	-	-	38	58
PE8	I/O	5T	SMC_D5, DMC_A4	TMR1_CH1N	-	-	39	59
PE9	I/O	5T	SMC_D6, DMC_A5	TMR1_CH1	-	-	40	60
V _{SS_7}	P	-	-	-	-	-	-	61
V _{DD_7}	P	-	-	-	-	-	-	62
PE10	I/O	5T	SMC_D7, DMC_A6	TMR1_CH2N	-	-	41	63
PE11	I/O	5T	SMC_D8, DMC_A7	TMR1_CH2	-	-	42	64
PE12	I/O	5T	SMC_D9, DMC_A8	TMR1_CH3N	-	-	43	65
PE13	I/O	5T	SMC_D10, DMC_A9	TMR1_CH3	-	-	44	66
PE14	I/O	5T	SMC_D11	TMR1_CH4	-	-	45	67
PE15	I/O	5T	SMC_D12, DMC_CLK	TMR1_BKIN	-	-	46	68
PB10	I/O	5T	I2C2_SCL, USART3_TX, DMC_UDQM	TMR2_CH3	21	29	47	69
PB11	I/O	5T	I2C2_SDA, USART3_RX, DMC_CKE	TMR2_CH4	22	30	48	70
V _{SS_1}	P	-	-	-	23	31	49	71
V _{DD_1}	P	-	-	-	24	32	50	72
PB12	I/O	5T	SPI2_NSS, I2S2_WS, I2C2_SMBAL, USART3_CK, TMR1_BKIN, CAN2_RX	-	25	33	51	73
PB13	I/O	5T	SPI2_SCK,	-	26	34	52	74

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
			I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX					
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, USART3_RTS	-	27	35	53	75
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N	-	28	36	54	76
PD8	I/O	5T	SMC_D13	USART3_TX	-	-	55	77
PD9	I/O	5T	SMC_D14	USART3_RX	-	-	56	78
PD10	I/O	5T	SMC_D15	USART3_CK	-	-	57	79
PD11	I/O	5T	SMC_A16	USART3_CTS	-	-	58	80
PD12	I/O	5T	SMC_A17	TMR4_CH1, USART3_RTS	-	-	59	81
PD13	I/O	5T	SMC_A18	TMR4_CH2	-	-	60	82
V _{SS_8}	P	-	-	-	-	-	-	83
V _{DD_8}	P	-	-	-	-	-	-	84
PD14	I/O	5T	SMC_D0	TMR4_CH3	-	-	61	85
PD15	I/O	5T	SMC_D1	TMR4_CH4	-	-	62	86
PG2	I/O	5T	SMC_A12	-	-	-	-	87
PG3	I/O	5T	SMC_A13	-	-	-	-	88
PG4	I/O	5T	SMC_A14	-	-	-	-	89
PG5	I/O	5T	SMC_A15	-	-	-	-	90
PG6	I/O	5T	SMC_INT2	-	-	-	-	91
PG7	I/O	5T	SMC_INT3	-	-	-	-	92
PG8	I/O	5T	-	-	-	-	-	93
V _{SS_9}	P	-	-	-	-	-	-	94
V _{DD_9}	P	-	-	-	-	-	-	95
PC6	I/O	5T	I2S2_MCK, TMR8_CH1, SDIO_D6	TMR3_CH1	-	37	63	96
PC7	I/O	5T	I2S3_MCK, TMR8_CH2,	TMR3_CH2	-	38	64	97

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
			SDIO_D7					
PC8	I/O	5T	TMR8_CH3, SDIO_D0	TMR3_CH3	-	39	65	98
PC9	I/O	5T	TMR8_CH4, SDIO_D1	TMR3_CH4	-	40	66	99
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO	-	29	41	67	100
PA9	I/O	5T	USART1_TX, TMR1_CH2	-	30	42	68	101
PA10	I/O	5T	USART1_RX, TMR1_CH3	-	31	43	69	102
PA11	I/O	5T	USART1_CTS, USBD1DM, USBD2DM, CAN1_RX, TMR1_CH4	-	32	44	70	103
PA12	I/O	5T	USART1_RTS, USBD1DP, USBD2DP, CAN1_TX, TMR1_ETR	-	33	45	71	104
PA13 (JTMS,SWDIO)	I/O	5T	-	PA13	34	46	72	105
NC	-	-	-	-	-	-	73	106
V _{SS_2}	P	-	-	-	35	47	74	107
V _{DD_2}	P	-	-	-	36	48	75	108
PA14 (JTCK,SWCLK)	I/O	5T	-	PA14	37	49	76	109
PA15 (JTDI)	I/O	5T	SPI3_NSS, I2S3_WS	TMR2_CH1_E TR,PA15, SPI1_NSS	38	50	77	110
PC10	I/O	5T	UART4_TX, SDIO_D2, DMC_DQ8	USART3_TX	-	51	78	111
PC11	I/O	5T	UART4_RX, SDIO_D3, DMC_DQ9	USART3_RX	-	52	79	112
PC12	I/O	5T	UART5_TX,	USART3_CK	-	53	80	113

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
			SDIO_CK					
PD0 (OSC_IN)	I/O	5T	SMC_D2	CAN1_RX	-	-	81	114
PD1 (OSC_OUT)	I/O	5T	SMC_D3	CAN1_TX	-	-	82	115
PD2	I/O	5T	TMR3_ETR, UART5_RX, SDIO_CMD, DMC_DQ10	-	-	54	83	116
PD3	I/O	5T	SMC_CLK, DMC_DQ11	USART2_CTS	-	-	84	117
PD4	I/O	5T	SMC_NOE, DMC_DQ12	USART2_RTS	-	-	85	118
PD5	I/O	5T	SMC_NWE, DMC_DQ13	USART2_TX	-	-	86	119
V _{SS_10}	P	-	-	-	-	-	-	120
V _{DD_10}	P	-	-	-	-	-	-	121
PD6	I/O	5T	SMC_NWAIT, DMC_DQ14	USART2_RX	-	-	87	122
PD7	I/O	5T	SMC_NE1, SMC_NCE2	USART2_CK	-	-	88	123
PG9	I/O	5T	SMC_NE2, SMC_NCE3, DMC_DQ15	-	-	-	-	124
PG10	I/O	5T	SMC_NCE4_1, SMC_NE3	-	-	-	-	125
PG11	I/O	5T	SMC_NCE4_2	-	-	-	-	126
PG12	I/O	5T	SMC_NE4, DMC_DQ0	-	-	-	-	127
PG13	I/O	5T	SMC_A24, DMC_DQ1	-	-	-	-	128
PG14	I/O	5T	SMC_A25, DMC_DQ2	-	-	-	-	129
V _{SS_11}	P	-	-	-	-	-	-	130
V _{DD_11}	P	-	-	-	-	-	-	131
PG15	I/O	5T	DMC_DQ3	-	-	-	-	132
PB3 (JTDO)	I/O	5T	SPI3_SCK, I2S3_CK	PB3, TRACESWO,	39	55	89	133

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	QFN48/L QFP48	LQFP6 4	LQFP10 0	LQFP14 4
				TMR2_CH2, SPI1_SCK				
PB4 (NJTRST)	I/O	5T	SPI3_MISO	PB4, TMR3_CH1, SPI1_MISO	40	56	90	134
PB5	I/O	STD	I2C1_SMBAL, SPI3_MOSI, I2S3_SD	TMR3_CH2, SPI1_MOSI, CAN2_RX	41	57	91	135
PB6	I/O	5T	I2C1_SCL, I2C3_SCL, TMR4_CH1	USART1_TX, CAN2_TX	42	58	92	136
PB7	I/O	5T	I2C1_SDA, I2C3_SDA, SMC_NADV, TMR4_CH2	USART1_RX	43	59	93	137
BOOT0	I	B	-	-	44	60	94	138
PB8	I/O	5T	TMR4_CH3, SDIO_D4	I2C1_SCL, I2C3_SCL, CAN1_RX	45	61	95	139
PB9	I/O	5T	TMR4_CH4, SDIO_D5	I2C1_SDA, I2C3_SDA, CAN1_TX	46	62	96	140
PE0	I/O	5T	TMR4_ETR, SMC_NBL0	-	-	-	97	141
PE1	I/O	5T	SMC_NBL1	-	-	-	98	142
V _{SS_3}	P	-	-	-	47	63	99	143
V _{DD_3}	P	-	-	-	48	64	100	144

Note:

- (1) The functions available depend on the selected model. For models with fewer peripheral modules, function modules with smaller numbers are always included. For example, when a model has only one SPI and two USARTs, they are SPI1, USART1 and USART2.
- (2) The PC13, PC14 and PC15 pins are powered by the power switch, which can only absorb a limited current (3mA). Therefore, when these three pins are used as output pins, there are the following restrictions: only one pin can be used as output at the same time, and when they are used as output pins, they can only work in 2MHz mode. The maximum driving load is 30pF, and they cannot be used as current sources (such as driving LED).
- (3) These pins are in the main function state when the backup area is powered on for the first time. After that, even if they are reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the relevant sections of the battery backup area and BAKPR register in the user manual.

- (4) This kind of multiplexing function can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O chapter and the debugging setting chapter of the user manual.
- (5) Pin 5 and pin 6 of LQFP64 and below package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. The software can reset these two pins as PD0 and PD1 functions. However, for LQFP100 package, since PD0 and PD1 are inherent function pins, it is unnecessary to re image by software. For more details, refer to the Reuse Function I/O section and the Debug Settings section of the reference manual. In output mode, PD0 and PD1 can only be configured as 50MHz output mode.

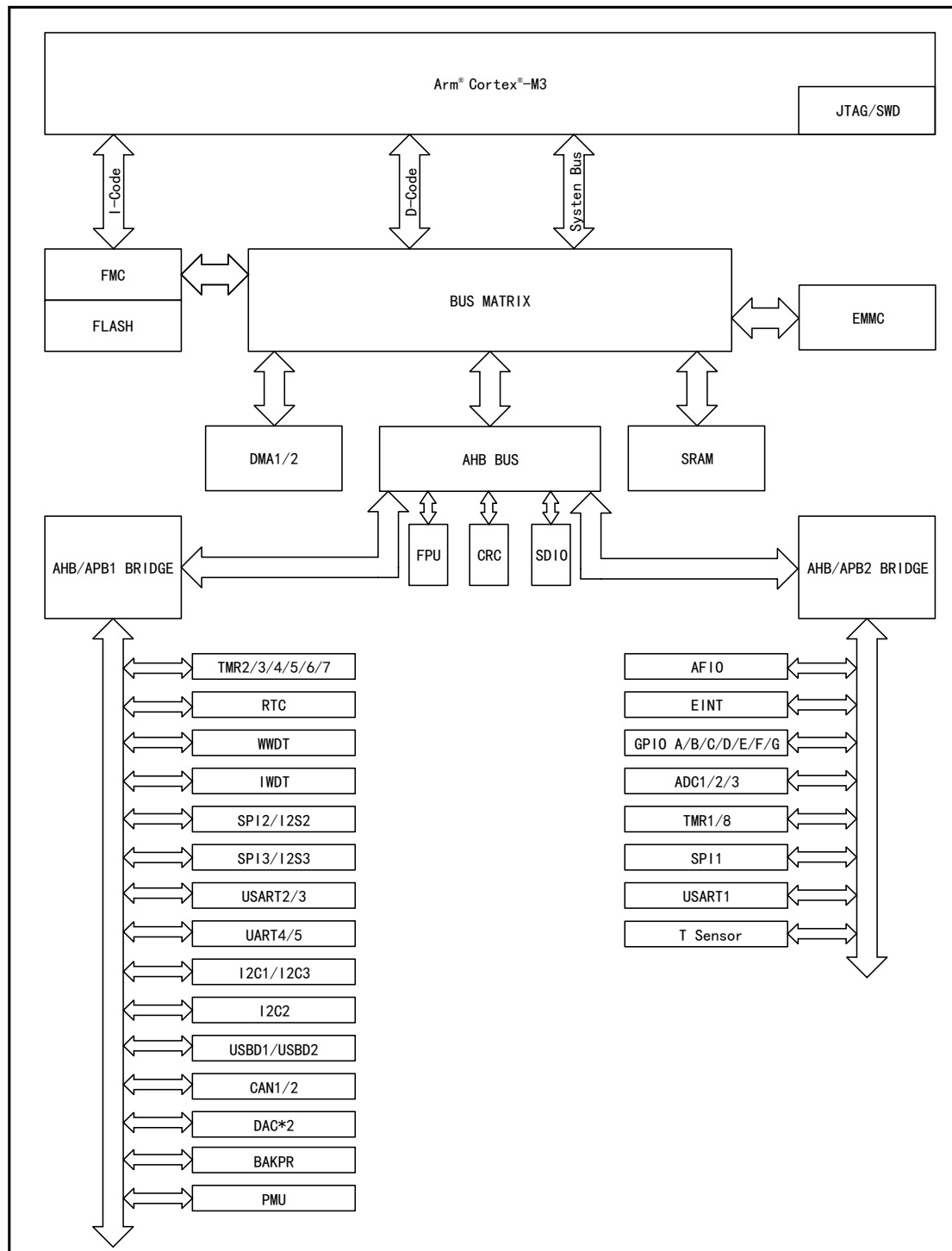
4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32E103xCxE series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

4.1. System architecture

4.1.1. System block diagram

Figure 6APM32E103xCxE System Block Diagram



4.1.2. Address mapping

Table 4 APM32E103xCxE Performance Line Address Mapping Diagram

Region	Start Address	Peripheral Name
Code	0x0000 0000	Mapping area
Code	0x0800 0000	Flash
Code	0x0808 0000	Reserved
Code	0x1FFF F000	System Memory
Code	0x1FFF F800	Option Bytes
Code	0x1FFF F810	Reserved
SRAM	0x2000 0000	SRAM
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	TMR5
APB1 bus	0x4000 1000	TMR6
APB1 bus	0x4000 1400	TMR7
APB1 bus	0x4000 1800	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	Reserved
APB1 bus	0x4000 3800	SPI2/I2S2
APB1 bus	0x4000 3C00	SPI3/I2S3
APB1 bus	0x4000 4000	Reserved
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	USART4
APB1 bus	0x4000 5000	USART5
APB1 bus	0x4000 5400	I2C1(I2C3)
APB1 bus	0x4000 5800	I2C2
APB1 bus	0x4000 5C00	USB1(USB2)
APB1 bus	0x4000 6000	USB/CAN SRAM
APB1 bus	0x4000 6400	CAN
APB1 bus	0x4000 6800	Reserved

Region	Start Address	Peripheral Name
APB1 bus	0x4000 6C00	BAKPR
APB1 bus	0x4000 7000	PMU
APB1 bus	0x4000 7400	DAC
—	0x4000 7800	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D
APB2 bus	0x4001 1800	Port E
APB2 bus	0x4001 1C00	Port F
APB2 bus	0x4001 2000	Port G
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	TMR8
APB2 bus	0x4001 3800	USART1
APB2 bus	0x4001 3C00	ADC3
—	0x4001 4000	Reserved
AHB bus	0x4001 8000	SDIO
AHB bus	0x4001 8400	Reserved
AHB bus	0x4002 0000	DMA1
AHB bus	0x4002 0400	DMA2
AHB bus	0x4002 0400	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash Interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x4002 4000	FPU

Region	Start Address	Peripheral Name
AHB bus	0x0002 4400	Reserved
AHB bus	0x6000 0000	EMMC bank 1 NOR/PSRAM 1/SDRAM
AHB bus	0x6400 0000	EMMC bank 1 NOR/PSRAM 2/SDRAM
AHB bus	0x6800 0000	EMMC bank 1 NOR/PSRAM 3/SDRAM
AHB bus	0x6C00 0000	EMMC bank 1 NOR/PSRAM 4/SDRAM
AHB bus	0x7000 0000	EMMC bank 2 NAND(NAND1)
AHB bus	0x8000 0000	EMMC bank 3 NAND(NAND2)
AHB bus	0x9000 0000	EMMC bank 4 PCCARD
AHB bus	0xA000 0000	EMMC Register
—	0xA000 1000	Reserved
Core	0xE000 0000	M3 Core peripheral

Note: SDRAM is directly addressed to 256M, without Bank access separately.

4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32E103xCxE is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 65 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information

block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table5 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	512 KB	Store user programs and data.
SRAM	128 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	2KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.4.1. External Memory Controller (EMMC)

EMMC includes SMC (static memory controller) and DMC (dynamic memory controller). SMC is responsible for controlling SRAM, PSRAM, NandFlash, NorFlash and PCCard; DMC is responsible for controlling SDRAM.

Function:

- Three EMMC interrupt sources, through logic or connected to the NVIC list
- Write FIFO
- Code could run on external storage besides NAND Flash and PC card
- Connect with LCD

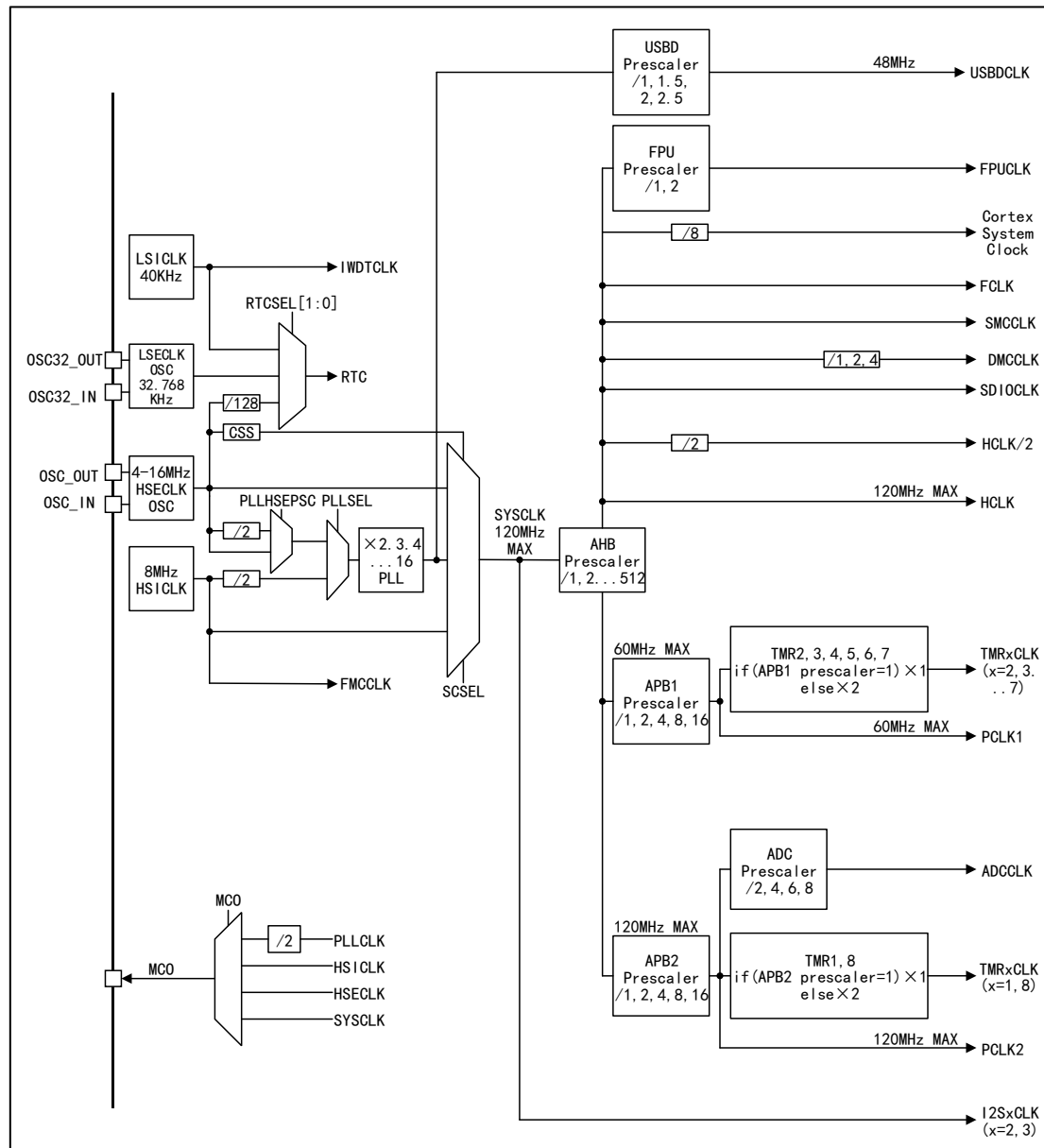
4.4.2. LCD parallel interface

EMMC can be configured to the seamless connection with most graphic LCD controller, it supports the Intel 8080 and Motorola 6800 model, and can be flexibly with specific LCD interface. Using the parallel interface LCD can be easily build simple graphics applications, or use a special scheme of high performance speed controller.

4.5. Clock

Clock tree of APM32E103xCxE is shown in the figure below:

Figure 7 APM32E103xCxE Clock Tree



4.5.1. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HS1CLK and HSECLK, and the low-speed clock includes LSECLK and LS1CLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HS1CLK and LS1CLK, and the external clock includes HSECLK and LSECLK, among which HS1CLK is calibrated by the factory to $\pm 1\%$ accuracy.

4.5.2. System clock

HS1CLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HS1CLK and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HS1CLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HS1CLK, and if an

interrupt is enabled, the software can receive the related interrupt.

4.5.3. Bus clock

AHB, APB1 and APB2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 120MHz, and the maximum frequency of APB1 is 60MHz.

4.6. Power supply and power management

4.6.1. Power supply scheme

Table 6 Power Supply Scheme

Name	Voltage range	Instruction
V _{DD}	2.0~3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V _{DD} pin.
V _{DDA} /V _{SSA}	2.0~3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V _{DDA} shall not be less than 2.4V; V _{DDA} and V _{SSA} must be connected to V _{DD} and V _{SS} .
V _{BAT}	1.8~3.6V	When V _{DD} is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch.

4.6.2. Voltage regulator

Table 7 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value (V_{POR/PDR}), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32E103xCxE supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 8 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.3V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBDM.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.3V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDG reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8. DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash, SRAM, SDRAM)

4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input, output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10. Communication peripherals

4.10.1. USART/UART

Up to 5 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 2.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; except UART5, all the other USART/UART can support DMA. USART/UART function differences are shown in the table below:

Table 9 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5
Hardware flow control of modem	√	√	√	—	—
Synchronous mode	√	√	√	√	√
Smart card mode	√	√	√	—	—
IrDASIR coder-encoder functions	√	√	√	√	√
LIN mode	√	√	√	√	√

USART mode/function	USART1	USART2	USART3	UART4	UART5
Single-line half-duplex mode	√	√	√	√	√
Support DMA function	√	√	√	√	—

Note: √ = support.

4.10.2. I2C

I2C1/2 and I2C3 bus interfaces are built in. I2C1 and I2C3 share hardware interface and register base address. Therefore, I2C1 and I2C3 cannot be used at the same time.

I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

I2C3 bus can operate in standard mode, fast mode and high-speed mode. The devices in high-speed mode and fast mode are downward compatible.

4.10.3. SPI/I2S

Three built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

4.10.4. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 28 3-level adjustable filters.

4.10.5. USB

The product embeds USB modules (USB1 and USB2) compatible with full-speed USB devices, which comply with the standard of full-speed USB devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USB is directly generated by internal PLL. When using the USB function, the system clock can only be one of 48MHz, 72MHz, 96MHz and 120MHz, which can obtain 48MHz required for USB through 1 fractional frequency, 1.5 fractional frequency, 2 fractional frequency and 2.5 fractional frequency respectively.

USB1 and USB2 share register address and pin interface, so only one of them can be used at the same time.

4.10.6. Simultaneous use of USB and CAN interfaces

This product USB1 (2) and CAN1 (2) sharing the same dedicated 512 - byte SRAM memory used to send and receive data, USB and CAN therefore be ready to use at the same time. Details are as follows:

- CAN1 and USB2 could be used at the same time

- CAN2 and USBD1 could be used at the same time
- USBD1 and USBD2 could not be used at the same time
- CAN1 and CAN2 could be used at the same time

Note: Although there are actually 2 identical USBDs (with the same pins), they can't be used together, so it's equivalent to only 1. Users can achieve "simultaneous use" by remapping (reuse of pins).

4.11. Analog peripherals

4.11.1. ADC

3 built-in ADCs with 12-bit accuracy, up to 21 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. ADC1 and ADC2 have 16 external channels, ADC3 generally has 8 external channels; A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

4.11.1.1. Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2. Internal reference voltage

Built-in reference voltage V_{REFINT} , internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.2. DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.12. Timer

2 built-in 16-bit advanced timers (TMR1/8), 4 general-purpose timers (TMR2/3/4/5), 2 basic timers (TMR6/7), 1 independent watchdog timer, one window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 10 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	Basic timer		General-purpose timer				Advanced timer	
Timer name	Sys Tick Timer	TMR6	TMR7	TMR2	TMR3	TMR4	TMR5	TMR1	TMR8
Counter resolution	24-bit	16 bits		16 bits				16 bits	
Counter type	Down	Up		Up, down, up/down				Up, down, up/down	

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
Prescaler coefficient	-	Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536
General DMA request	-	OK	OK	OK
Capture/Comparison channel	-	-	4	4
Complementary outputs	-	No	No	Yes
Pin characteristics	-	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins	There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter.	Synchronization or event chaining function provided Timers in debug mode can be frozen. -Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals	It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 11 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems.

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
				Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN and OSC32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.13.1. Backup register

84Bytes backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

4.15. FPU

The product has built-in independent FPU floating-point operation processing unit, supports IEEE754 standard, supports single-precision floating-point operation, and supports algorithms such as CMP, SUM, SUB, PRDCT, MAC, DIV, INVRGSQT, RGSQT, SUMSQ, DOT, floating-point to integer conversion and integer to floating point conversion.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at $T_A=25^{\circ}\text{C}$. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average $\pm 3\Sigma$) to get the maximum and minimum values.

5.1.2. Typical value

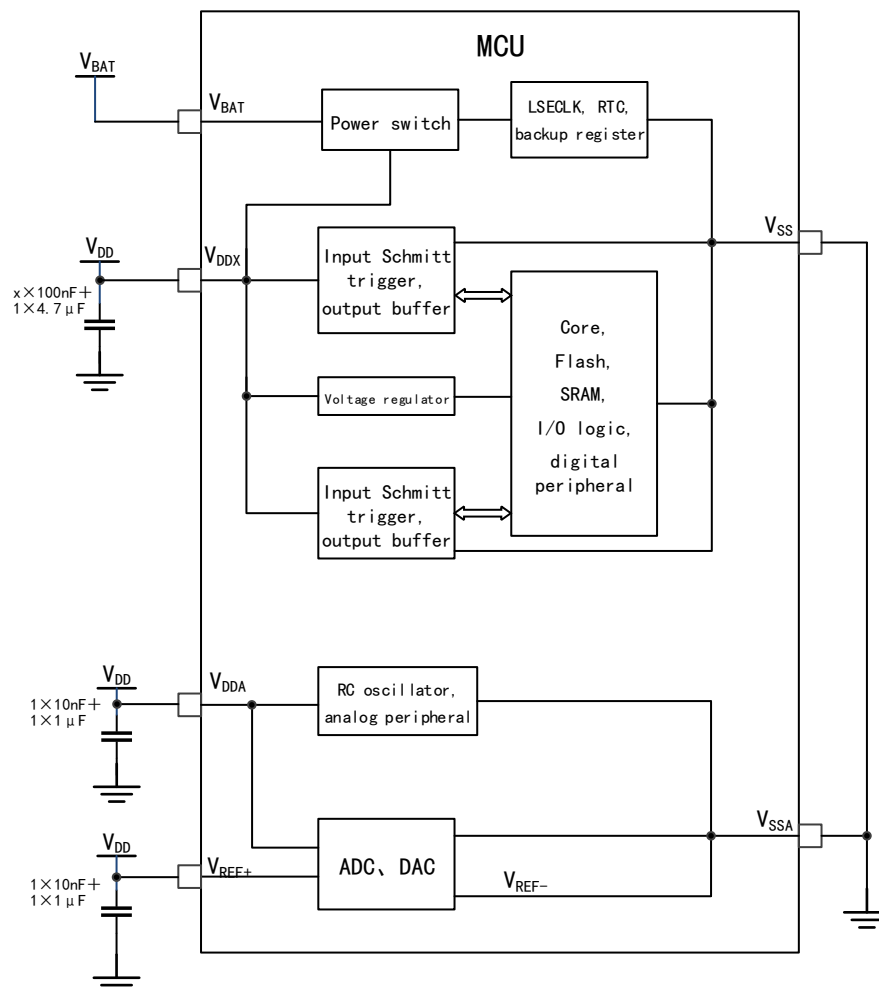
Unless otherwise specified, typical data are measured based on $T_A=25^{\circ}\text{C}$, $V_{DD}=V_{DDA}=3.3\text{V}$. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 8 Power Supply Scheme



Notes: V_{DDX} in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 9 Load conditions when measuring pin parameters

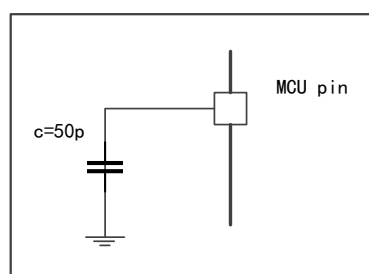


Figure 10 Pin Input Voltage Measurement Scheme

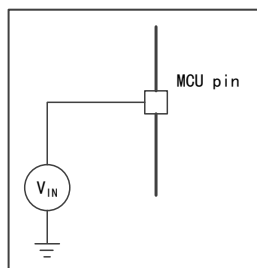
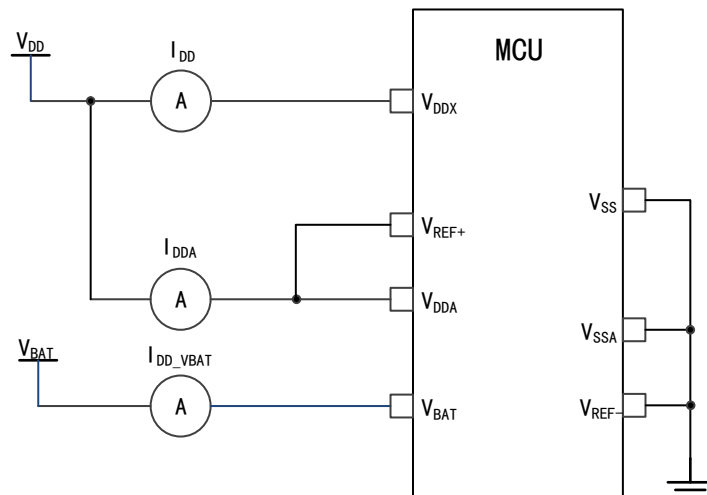


Figure 11 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table 12 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency	-	-	120	MHz
f _{PCLK1}	Internal APB1 clock frequency	-	-	60	
f _{PCLK2}	Internal APB2 clock frequency	-	-	120	
V _{DD}	Main power supply voltage	-	2	3.6	V
V _{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V _{DD}	V _{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V _{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T _A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	°C
	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	°C

Note: During power-up and normal operation, it is recommended to use the same power supply for V_{DD} and V_{DDA}, with a maximum voltage difference of 300 mV between V_{DD} and V_{DDA}.

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 13 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	°C
T_J	Maximum junction temperature	150	°C

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 14 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
$V_{DD} - V_{SS}$	External main power supply voltage	-0.3	4.0	V
$V_{DDA} - V_{SSA}$	External analog power supply voltage	-0.3	4.0	
$V_{BAT} - V_{SS}$	Power supply voltage of external backup domain	-0.3	4.0	
$ V_{DD} - V_{DDA} $	Voltage difference allowed by $V_{DD} > V_{DDA}$	-	0.3	
V_{IN}	Input voltage on FT pins	$V_{SS} - 0.3$	5.5	
	Input voltage on other pins	$V_{SS} - 0.3$	$V_{DD} + 0.3$	mV
$ \Delta V_{DDx} $	Voltage difference between different power supply pins	-	50	
$ V_{SSx} - V_{SS} $	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current features

Table 15 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}^{(2)(3)}$	Injection current of 5T pin	-5	
	Injection current of other pins	±5	
$\Sigma I_{INJ(PIN)}^{(2)}$	Total injection current on all I/O and control pins ⁽⁴⁾	±25	

- (1) All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to a power supply within the external allowable range.
- (2) Negative injection disturbs the analog performance of the device.
- (3) Positive injection is not possible on these I/Os. a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
- (4) A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
- (5) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4. Electrostatic discharge (ESD)

Table 16 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^{\circ}\text{C}$	± 5000	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table 17 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	$T_A = +25\text{ }^{\circ}\text{C}/105^{\circ}\text{C}$, conforming to EIA/JESD78E	CLASS II A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table 18 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	$T_A = -40\sim 105^{\circ}\text{C}$ $V_{DD}=2.4\sim 3.6\text{V}$	40	46.08	70	μs
t_{ERASE}	Page (2KBytes) erase time	$T_A = -40\sim 105^{\circ}\text{C}$ $V_{DD}=2.4\sim 3.6\text{V}$	10	-	30	ms
t_{ME}	Whole erase time	$T_A = 40\sim 105^{\circ}\text{C}$ $V_{DD}=3.3\text{V}$	10	-	30	ms
V_{prog}	Programming voltage	$T_A = -40\sim 105^{\circ}\text{C}$	2	-	3.6	V
t_{RET}	Data saving time	$T_A=125^{\circ}\text{C}$	10.77	-	-	years
N_{RW}	Erase cycle	$T_A=85^{\circ}\text{C}$	100K	-	-	cycles

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 HSECLK4~16MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
RF	Feedback resistance	-	-	200	-	kΩ
I _{DD(HSECLK)}	HSECLK current consumption	V _{DD} =3.3V, CL=10pF@8MHz	-	-	0.56	mA
t _{SU(HSECLK)}	Startup time	V _{DD} is stable	-	0.85	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 20 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f _{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
I _{DD(LSECLK)}	LSECLK current consumption	-	-	-	0.8	μA
t _{SU(LSECLK)} ⁽¹⁾	Startup time	V _{DDIOx} is stable	-	0.93	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

- (1) t_{SU(LSECLK)} is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

High speed internal (HSICLK) RC oscillator

Table 21 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f _{HSICLK}	Frequency	-	-	8	-	MHz
A _{ACC(HSICLK)}	Accuracy of HSICLK oscillator	Factory calibration. T _A =25°C	-1	-	1	%

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		$T_A = -10 \sim 85^{\circ}\text{C}$	-2.5		2.5	%
		$T_A = -40 \sim 105^{\circ}\text{C}$	-5	-	2.5	%
$I_{DDA}(\text{HSICLK})$	Power consumption of HSICLK oscillator	-	-	-	76	μA
$t_{\text{SU}}(\text{HSICLK})$	Startup time of HSICLK oscillator	$V_{DD}=3.3\text{V}$, $T_A=-40 \sim 105^{\circ}\text{C}$	3.24	-	3.4	μs

Note: It is obtained from the design guarantee and is not tested in production. Deviations may occur after long time usage, but the maximum range specified above can still be ensured.

Low speed internal (LSICLK) RC oscillator

Table 22 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency ($V_{DD}=2\sim 3.6\text{V}$, $T_A=-40 \sim 105^{\circ}\text{C}$)	30	40	60	KHz
$I_{DD}(\text{LSICLK})$	Power consumption of LSICLK oscillator	-	-	0.56	μA
$t_{\text{SU}}(\text{LSICLK})$	LSICLK oscillator startup time, ($V_{DD}=3.3\text{V}$, $T_A=-40 \sim 105^{\circ}\text{C}$)	-	-	74.8	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table 23 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical value	Maximum value	
$f_{\text{PLL_IN}}$	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
$f_{\text{PLL_OUT}}$	PLL frequency doubling output clock, ($V_{DD}=3.3\text{V}$, $T_A=-40 \sim 105^{\circ}\text{C}$)	16	-	120	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Power-on/power-down characteristics

Table 24 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	1	-	200000	$\mu\text{s/V}$
	V_{DD} fall time rate		1	-	200000	

5.6.2. Test of embedded reset and power control block characteristics

Table 25 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{POR/PDR}	Power-on/power-down reset threshold	Falling edge	1.84	1.86	1.88	V
		Rising edge	1.90	1.92	1.93	V
V _{PDRhyst}	PDR hysteresis	-	50.00	54.00	60.00	mV
T _{RSTTEMPO}	Reset duration	-	0.90	1.39	4.90	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 26 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.17	-	2.20	V
		PLS[2:0]=000 (falling edge)	2.06	-	2.10	V
		PLS[2:0]=000(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=001 (rising edge)	2.27	-	2.30	V
		PLS[2:0]=001 (falling edge)	2.16	-	2.19	V
		PLS[2:0]=001(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=010 (rising edge)	2.37	-	2.40	V
		PLS[2:0]=010 (falling edge)	2.26	-	2.29	V
		PLS[2:0]=010(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=011 (rising edge)	2.46	-	2.50	V
		PLS[2:0]=011 (falling edge)	2.36	-	2.39	V
		PLS[2:0]=011(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=100 (rising edge)	2.57	-	2.60	V
		PLS[2:0]=100 (falling edge)	2.45	-	2.49	V
		PLS[2:0]=100(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edge)	2.66	-	2.70	V
		PLS[2:0]=101 (falling edge)	2.56	-	2.59	V
		PLS[2:0]=101(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=110 (rising edge)	2.76	-	2.80	V
		PLS[2:0]=110 (falling edge)	2.65	-	2.69	V
		PLS[2:0]=110(PVD hysteresis)	110	-	110	mV
		PLS[2:0]=111 (rising edge)	2.87	-	2.91	V
		PLS[2:0]=111 (falling edge)	2.75	-	2.79	V

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=111(PVD hysteresis)	110	-	120	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

Forms containing SDRAM are applicable to APM32E103xCxETxS, otherwise applicable to APM32E103xCxETx.

5.7.1. Power consumption test environment

- (1) The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.
- (2) All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- (3) Unless otherwise specified, all peripherals are turned off
- (4) The relationship between Flash waiting cycle setting and f_{HCLK} :
 - 0~24MHz: 0 waiting cycle
 - 24~48MHz: 1 waiting cycle
 - 48~72MHz: 2 waiting cycles
 - 72~96MHz: 3 waiting cycles
 - 96~120MHz: 4 waiting cycles
- (5) The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)
- (6) When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table 27 Power Consumption in Run Mode when the Program is Executed in Flash

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
Power consumption in run mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	96MHz	218.17	20.90	257.25	22.75
		72MHz	152.43	15.01	183.55	16.77
		48MHz	121.33	12.42	148.55	14.07
		36MHz	98.50	9.43	120.42	11.23
		24MHz	121.30	6.93	144.77	8.34
		16MHz	91.31	4.83	111.79	6.37
		8MHz	17.84	2.78	27.24	4.31
	HSECLK bypass ⁽²⁾ , turning off all peripherals	96MHz	217.99	11.61	253.19	12.85
		72MHz	152.30	8.93	179.31	10.31
		48MHz	121.29	7.70	144.81	9.00
		36MHz	98.48	5.94	119.48	7.32
		24MHz	121.24	4.53	144.81	5.85
		16MHz	91.24	3.26	111.79	4.56
		8MHz	17.84	1.98	26.08	3.30
	HSICLK ⁽²⁾ , enabling all peripherals	64MHz	237.41	15.13	274.23	16.00
		48MHz	206.64	11.06	241.56	12.85
		36MHz	184.46	8.96	218.40	10.49
		24MHz	163.22	6.47	197.36	7.99
		16MHz	177.22	4.53	210.87	6.22
		8MHz	102.67	2.43	131.44	3.98
	HSICLK ⁽²⁾ , turning off all peripherals	64MHz	237.26	8.30	272.66	9.93
		48MHz	206.69	6.48	240.48	8.09
		36MHz	184.47	5.51	217.58	6.78
		24MHz	163.15	4.10	196.21	5.33
		16MHz	177.19	2.91	210.01	4.56
		8MHz	102.67	1.61	131.14	3.46

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 28 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
Power consumption in run mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	96MHz	218.11	18.82	254.07	19.78
		72MHz	168.27	14.51	198.01	15.31
		48MHz	121.38	10.23	145.28	11.22
		36MHz	98.49	7.91	119.64	8.85
		24MHz	121.37	5.75	145.12	6.69
		16MHz	91.32	4.23	111.49	5.54
		8MHz	17.85	2.22	26.07	3.37
	HSECLK bypass ⁽²⁾ , turning off all peripherals	96MHz	218.15	12.98	253.06	13.84
		72MHz	168.21	10.19	197.29	10.91
		48MHz	121.37	7.19	144.47	8.23
		36MHz	98.45	5.76	119.07	6.70
		24MHz	121.38	4.27	144.40	5.33
		16MHz	91.31	3.28	111.54	4.37
		8MHz	17.84	2.23	25.98	3.37
	HSICLK ⁽²⁾ , enabling all peripherals	64MHz	237.31	13.98	272.39	15.31
		48MHz	206.81	10.51	239.84	12.06
		36MHz	184.48	8.14	216.88	9.59
		24MHz	163.22	5.41	195.99	6.97
		16MHz	177.24	3.61	209.78	5.25
		8MHz	102.72	1.89	130.84	3.45
	HSICLK ⁽²⁾ , turning off all peripherals	64MHz	237.31	7.79	272.15	9.41
		48MHz	206.70	5.97	239.51	7.38
		36MHz	184.51	4.29	216.97	6.33
		24MHz	163.17	2.96	196.29	4.53
		16MHz	177.19	2.06	209.49	3.79
		8MHz	102.68	1.10	130.88	2.92

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table 29 Power Consumption in Sleep Mode when the Program is Executed in Flash

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
Power consumption in sleep mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	96 MHz	218.32	14.26	254.68	15.10
		72MHz	152.47	9.76	180.70	10.58
		48MHz	121.43	7.47	145.37	8.33
		36MHz	98.48	5.80	119.78	6.79
		24MHz	121.32	4.11	145.35	5.03
		16MHz	91.28	2.94	112.16	3.97
		8MHz	17.84	1.70	25.92	2.69
	HSECLK bypass ⁽²⁾ , turning off all peripherals	96 MHz	217.98	3.23	254.24	4.08
		72MHz	152.21	2.35	180.39	3.29
		48MHz	121.22	1.92	146.02	2.87
		36MHz	98.38	1.59	119.88	2.58
		24MHz	121.23	1.27	145.50	2.28
		16MHz	91.20	1.05	112.22	2.04
		8MHz	17.81	0.78	25.89	1.75
	HSICLK ⁽²⁾ , enabling all peripherals	64MHz	237.16	9.60	265.57	9.76
		48MHz	206.68	6.92	232.79	7.61
		36MHz	184.45	5.30	209.44	5.83
		24MHz	163.15	3.65	187.49	4.21
		16MHz	177.10	2.53	201.95	3.10
		8MHz	102.66	1.32	122.81	1.93
	HSICLK ⁽²⁾ , turning off all peripherals	64MHz	237.18	1.90	266.22	2.52
		48MHz	206.62	1.48	233.01	2.10
		36MHz	184.34	1.17	209.43	1.79
		24MHz	163.05	0.84	187.62	1.50
		16MHz	177.13	0.62	202.01	1.27
		8MHz	102.67	0.35	122.81	1.02

Table 30 Power Consumption in Sleep Mode when the Program is Executed in RAM

Parameter	Conditions	f_{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			$T_A=25^{\circ}C, V_{DD}=3.3V$		$T_A=105^{\circ}C, V_{DD}=3.6V$	
			$I_{DDA}(\mu A)$	$I_{DD}(mA)$	$I_{DDA}(\mu A)$	$I_{DD}(mA)$
Power consumption in sleep mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	96MHz	215.97	14.06	250.92	15.59
		72MHz	165.85	10.84	196.02	10.74
		48MHz	119.17	7.44	142.13	7.71
		36MHz	96.50	5.77	117.08	5.84
		24MHz	119.21	3.93	136.05	4.35
		16MHz	89.36	2.77	109.38	3.14
		8MHz	17.73	1.6	23.65	2.01
	HSECLK bypass ⁽²⁾ , turning off all peripherals	96MHz	215.53	3.12	248.57	3.64
		72MHz	165.75	2.44	192.92	3.14
		48MHz	118.99	1.80	141.57	2.24
		36MHz	96.46	1.44	117.39	1.94
		24MHz	119.11	1.15	142.46	1.63
		16MHz	89.21	0.94	109.67	1.36
		8MHz	17.71	0.66	23.00	1.14
	HSICLK ⁽²⁾ , enabling all peripherals	64MHz	237.15	9.31	265.75	9.74
		48MHz	206.68	7.13	232.94	7.56
		36MHz	184.39	5.44	209.27	5.87
		24MHz	163.18	3.51	187.51	4.27
		16MHz	177.19	2.45	201.95	3.12
		8MHz	102.68	1.28	122.82	1.91
	HSICLK ⁽²⁾ , turning off all peripherals	64MHz	237.19	1.93	266.13	2.54
		48MHz	206.65	1.47	233.12	2.10
		36MHz	184.36	1.13	209.35	1.80
		24MHz	163.10	0.82	187.67	1.50
		16MHz	177.13	0.62	202.00	1.29
		8MHz	102.60	0.36	122.86	1.03

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when $f_{HCLK}>8MHz$, turn on PLL, otherwise, turn off PLL

5.7.4. Power consumption in stop mode and standby mode

Table 31 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value ⁽¹⁾ , (T _A =25°C)						Maximum value ⁽¹⁾ , (V _{DD} =3.6V)		Unit
		V _{DD} =2.4V		V _{DD} =3.3V		V _{DD} =3.6V		T _A =105°C		
		I _{DDA}	I _{DD}	I _{DDA}	I _{DD}	I _{DDA}	I _{DD}	I _{DDA}	I _{DD}	
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.658	43.12	4.308	42.15	4.719	43.18	7.421	614.478	μA
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.667	36.77	4.324	36.69	4.695	37.13	7.039	552.132	
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.911	0.47	3.85	1.01	4.342	1.31	5.937	5.468	
	Low-speed internal RC oscillator on, independent watchdog OFF	2.919	0.27	3.846	0.75	4.336	1.15	5.918	4.587	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.346	0.05	2.964	0.17	3.343	0.40	4.985	4.172	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table 32 Backup Domain Power Consumption

Symbol	Conditions	Typical value ⁽¹⁾ , T _A =25°C			Maximum value ⁽¹⁾ , V _{BAT} =3.6V			Unit
		V _{BAT} =2.0V	V _{BAT} =2.4V	V _{BAT} =3.3V	T _A =25°C	T _A =85°C	T _A =105°C	
I _{DD_VBAT}	The low-speed oscillator and RTC are in ON state	1.106	1.268	1.704	1.956	2.568	3.256	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 33 Peripheral Power Consumption

Parameter	Peripheral	Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V	Unit
AHB	DMA1	0.3	mA
	DMA2	0.34	
	EMMC	0.31	

Parameter	Peripheral	Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V	Unit
	CRC	0.14	
	SDIO	0.52	
APB1	TMR2	0.25	
	TMR3	0.24	
	TMR4	0.4	
	TMR5	0.36	
	TMR6	0.06	
	TMR7	0.08	
	WWDT	0.04	
	IWDT	0.07	
	SPI2/I2S2	0.2	
	SPI3/I2S3	0.29	
	USART2	0.36	
	USART3	0.33	
	UART4	0.16	
	UART5	0.2	
	I2C1	0.22	
	I2C2	0.18	
	USB	0.42	
	CAN1	0.25	
	CAN2	0.25	
	BAKPR	0.02	
	PMU	0.02	
	DAC	0.16	
APB2	GPIOA	0.13	
	GPIOB	0.13	
	GPIOC	0.07	
	GPIOD	0.05	
	GPIOE	0.06	
	GPIOF	0.16	
	GPIOG	0.24	
	ADC1	0.39	
	ADC2	0.28	

Parameter	Peripheral	Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V	Unit
	ADC3	0.28	
	TMR1	0.4	
	TMR8	0.4	
	SPI1	0.13	
	USART1	0.2	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 34 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typical value (T _A =25°C)			Max	Unit
				2V	3.3V	3.6V		
t _{WUSLEEP}	Wake-up from sleep mode	-	0.52	0.61	0.60	0.57	0.65	μs
t _{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	1.83	2.24	1.91	1.86	2.26	
		The voltage regulator is in low power mode	2.66	4.18	2.95	2.82	4.61	
t _{WUSTDBY}	Wake up from standby mode	-	59.56	76.40	63.74	61.29	84.56	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table 35 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~105°C)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{IL}	Low level input voltage	CMOS port	-0.5	-	0.35V _{DD}	V
V _{IH}	High level input voltage		0.65V _{DD}	-	V _{DD} +0.5	
V _{IL}	Low level input voltage	TTL port	-0.5	-	0.8	
V _{IH}	High level input voltage, Standard I/O port		2	-	V _{DD} +0.5	
	High level input voltage, I/O FT port		2		5.5	
V _{hys}	Standard I/O Schmitt trigger voltage hysteresis	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%V _{DD}	-	-	mV
I _{lkg}	Input leakage current	V _{SS} ≤ V _{IN} ≤ V _{DD} Standard I/O port	-	-	±1	μA

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		$V_{IN}=5V$, I/O FT port	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	k Ω
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	30	40	50	k Ω

Note: It is obtained from a comprehensive evaluation and is not tested in production.

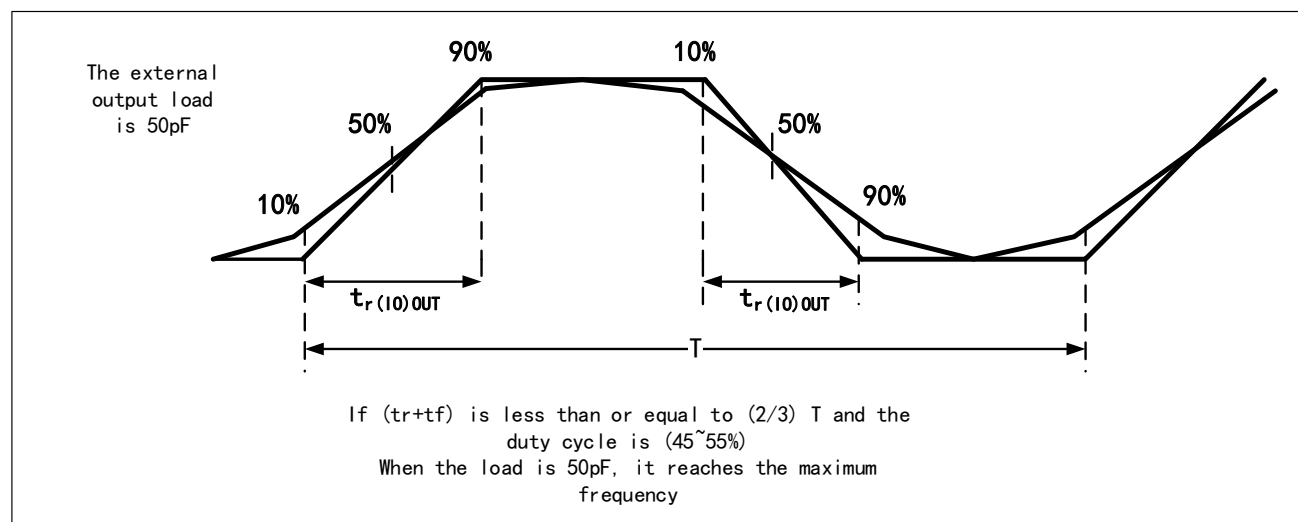
Table 36 AC Characteristics

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	fmax(IO)out	Maximum frequency	CL=50 pF, V _{DD} =2~3.6V	-	2	MHz
	tf(IO)out	Output fall time from high to low level	CL=50 pF, V _{DD} =2~3.6V	-	125	ns
	tr(IO)out	Output rise time from low to high level		-	125	
01 (10MHz)	fmax(IO)out	Maximum frequency	CL=50 pF, V _{DD} =2~3.6V	-	10	MHz
	tf(IO)out	Output fall time from high to low level	CL=50 pF, V _{DD} =2~3.6V	-	25	ns
	tr(IO)out	Output rise time from low to high level		-	25	
11 (50MHz)	fmax(IO)out	Maximum frequency	CL=30 pF, V _{DD} =2.7~3.6V	-	50	MHz
	tf(IO)out	Output fall time from high to low level	CL=30 pF, V _{DD} =2.7~3.6V	-	5	ns
	tr(IO)out	Output rise time from low to high level		-	5	

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 12 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table37 Output Drive Current Characteristics (test condition $V_{DD}=2.7\sim 3.6V$, $T_A=-40\sim 105^{\circ}C$)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +8mA$ $2.7V < V_{DD} < 3.6V$	-	0.49	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20mA$ $2.7V < V_{DD} < 3.6V$	-	1.50	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.2$	-	

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU} .

Table 38 NRST Pin Characteristics (test condition $V_{DD}=3.3V$, $T_A=-40\sim 105^{\circ}C$)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{IL}(NRST)$	NRST low level input voltage	-	-0.5	-	0.8	V
$V_{IH}(NRST)$	NRST high level input voltage	-	2	-	$V_{DD}+0.5$	
$V_{hys}(NRST)$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	30	40	50	k Ω

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

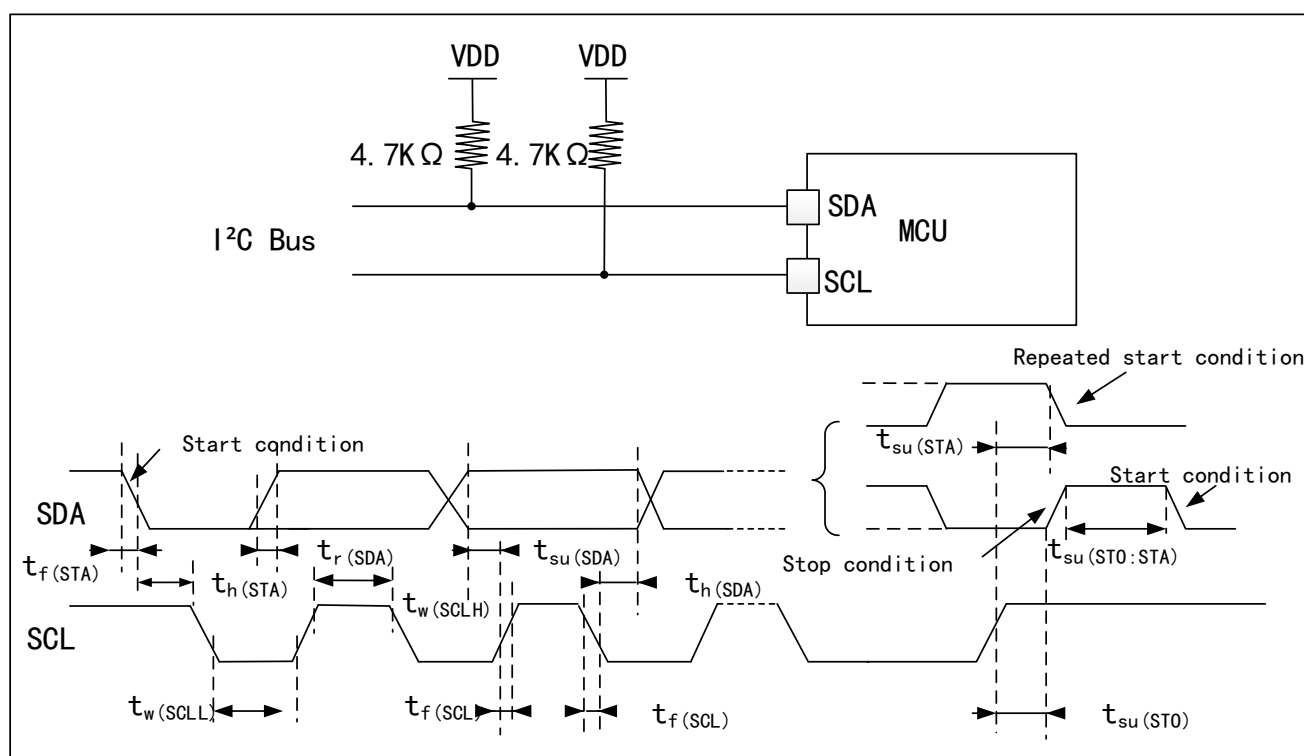
Table 39 I2C Interface Characteristics ($T_A=25^{\circ}C$, $V_{DD}=3.3V$)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_w(SCLL)$	SCL clock low time	4.7	-	1.3	-	μs
$t_w(SCLH)$	SCL clock high time	4.0	-	0.6	-	
$t_{su}(SDA)$	SDA setup time	250	-	100	-	ns
$t_h(SDA)$	SDA data hold time	-	3450	-	900	
$t_r(SDA)/t_r(SCL)$	SDA and SCL rise time	-	1000	-	300	
$t_f(SDA)/t_f(SCL)$	SDA and SCL fall time	-	300	-	300	
$t_h(STA)$	Start condition hold time	4.0	-	0.6	-	μs

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_w(STO:STA)$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 13 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table 40 SPI Characteristics ($T_A=25^\circ\text{C}$, $V_{DD}=3.3\text{V}$)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_c(SCK)$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: $C = 30\text{pF}$	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_w(SCKH)$	SCK high and low time	Main mode, $f_{PCLK} = 36\text{MHz}$,	50	60	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKL)}$		Prescaler coefficient=4			
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode Slave mode	5 5	- -	ns
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode Slave mode	5 4	- -	ns
$t_{a(SO)}$	Data output access time	Slave mode, $f_{PCLK} = 20MHz$	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	2	10	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$ $t_{h(MO)}$	Data output hold time	Slave mode (after enable edge) Master mode (after enable edge)	15 2	- -	ns

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 14 SPI Timing Diagram - Slave Mode and CPHA=0

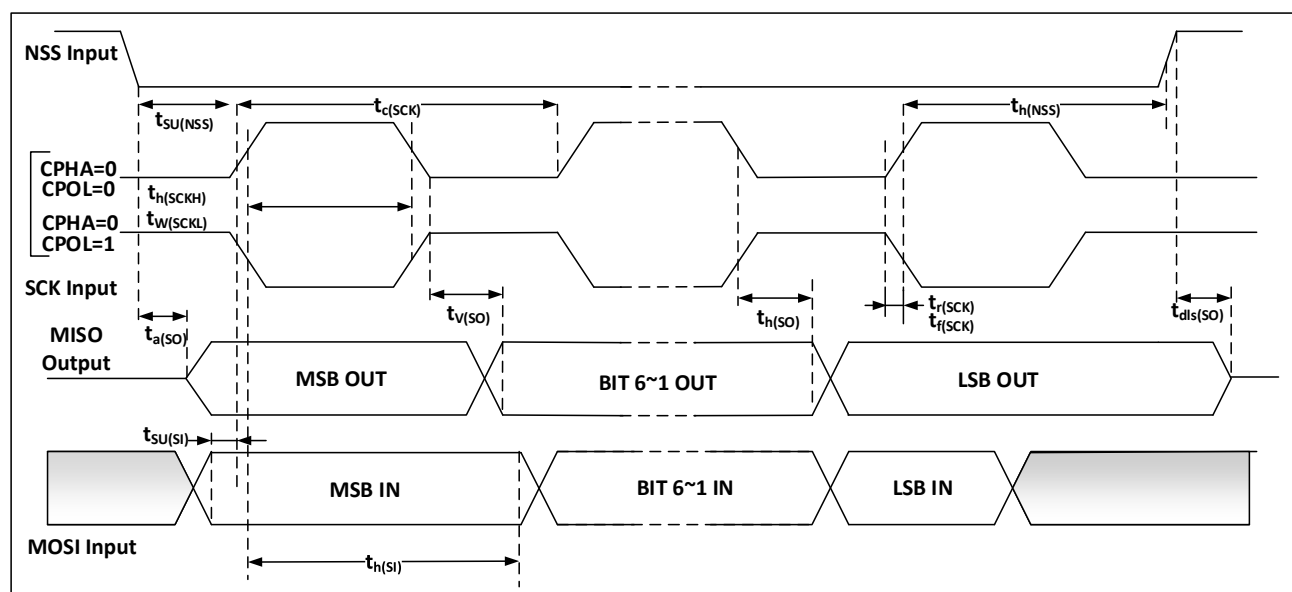
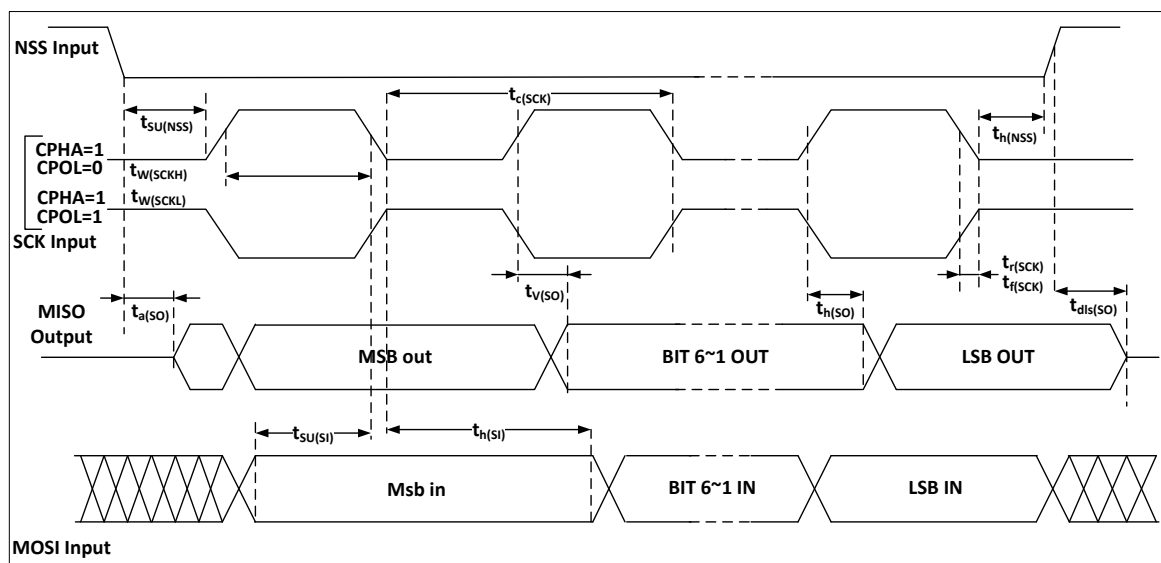
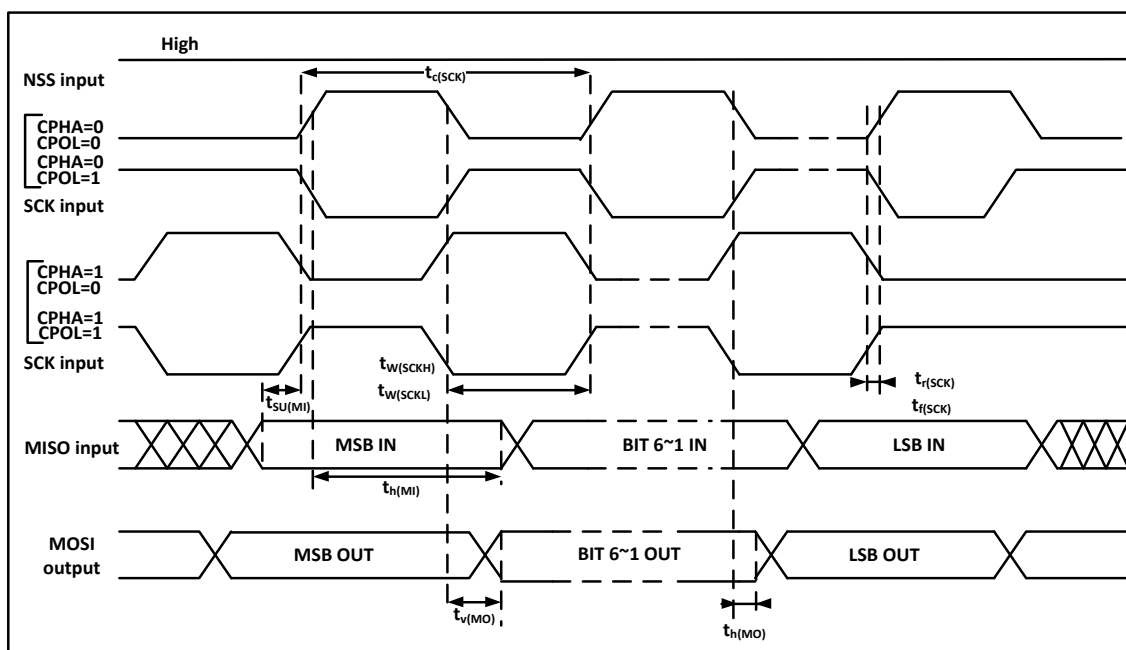


Figure 15 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 16 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversions of analog quantity to digital quantity by ADC per second
Sample rate = $\text{ADC clock} / (\text{number of sampling periods} + \text{number of conversion periods})$

5.11.1.1. 12-bit ADC characteristics

Table 41 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{DDA}	Power supply voltage	-	2.4	-	3.6	V
I _{DDA}	ADC power consumption	V _{DDA} =3.3V, f _{ADC} =14MHz, Sampling time=1.5 f _{ADC}	-	1	-	mA
f _{ADC}	ADC frequency	-	0.6	-	14	MHz
C _{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R _{ADC}	Sampling resistor	-	-	-	1000	Ω
t _s	Sample Time	f _{ADC} =14MHz	0.107	-	17.1	μs
T _{CONV}	Sampling and conversion time	f _{ADC} =14MHz, 12-bit conversion	1	-	18	μs

Table 42 12-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E _T	Total uncorrected error	f _{PCLK} =56MHz, f _{ADC} =14MHz, V _{DDA} =2.4V-3.6V T _A =-40°C~105°C	±2	±5	LSB
E _O	offset error		±1.5	±2.5	
E _G	Gain error		±1.5	±3	
E _D	Differential linear error		±1	±2	
E _L	Integral linearity error		±1.5	±3	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 43 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{REFINT}	Built-in Reference Voltage	-40°C < T _A < +105°C V _{DD} = 2-3.6 V	1.1882	1.1947	1.2002	V
T _{S_vrefint}	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V _{RERINT}	Built-in reference voltage extends to temperature range	V _{DD} =3V ±10mV	-	-	18	mV
T _{coeff}	Temperature coefficient	-	-	-	104	ppm/°C

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.3. Temperature Sensor

Table 44 Temperature Sensor Characteristics

Symbol	Parameters	Minimum Value	Typical Value	Maximum Value	Unit
Avg_Slope ⁽¹⁾	Average slope (V _{DD} = 3.3V, T _A = -40~105°C)	3.2	3.6	3.8	mV/°C
V ₂₅	Voltage at 25°C (V _{DD} = 2~3.6V)	1.42	1.46	1.48	V
t _{START} ⁽²⁾	Setup time	4	-	10	μs
T _{S_temp} ^{(2) (3)}	ADC sampling time when reading the temperature	-	-	17.1	μs

Note:

(1) Data is guaranteed from analysis results, and is not tested in production.

(2) Data is guaranteed from design, and is not tested in production.

(3) The shortest sampling Time can be determined by the application through multiple iterations.

5.11.2. DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is-1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 45 DAC Characteristics

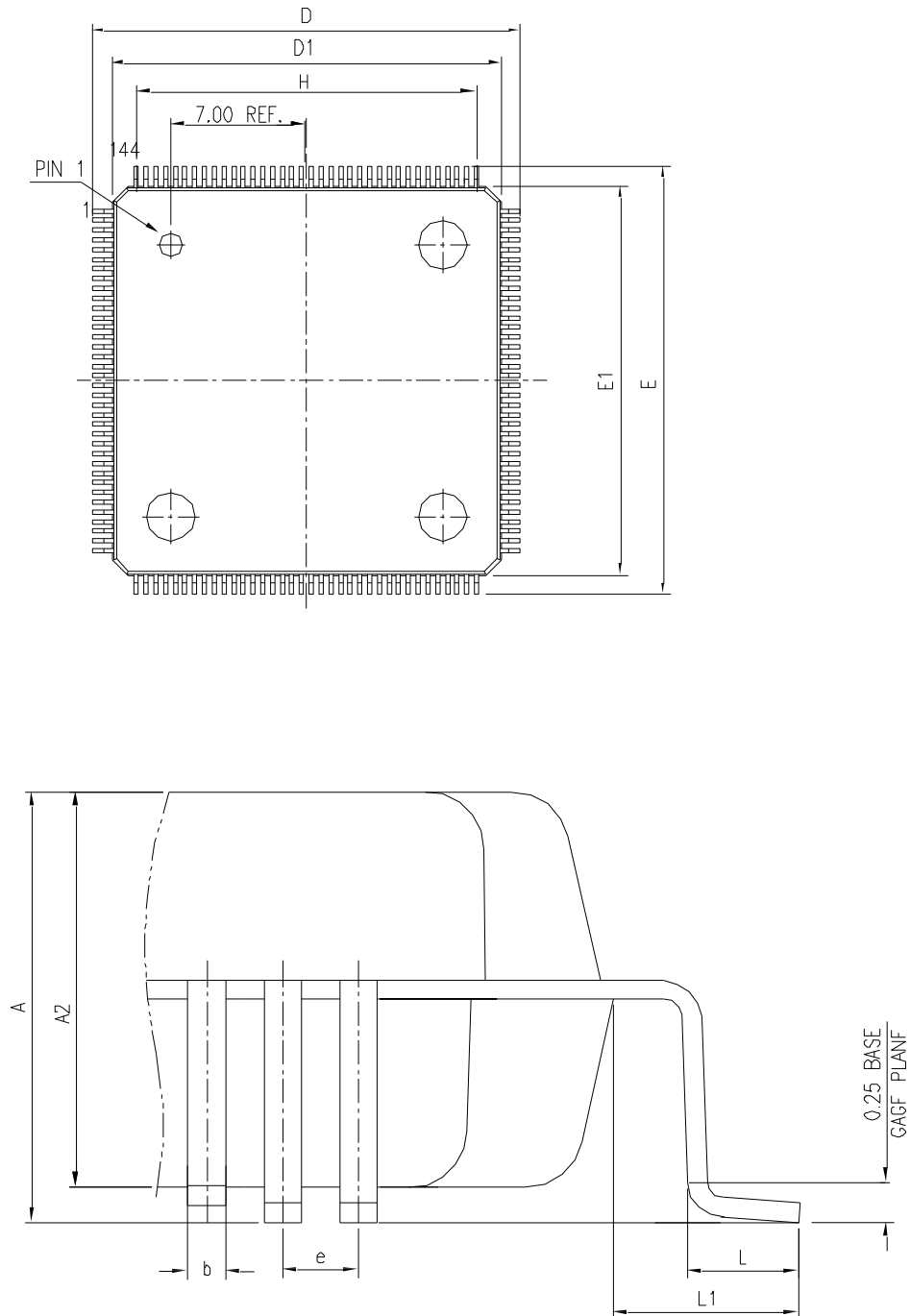
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V _{DDA}	Analog power supply voltage	-	2.4	-	3.6	V
R _{LOAD}	Resistive load	Load is connected to VSSA with buffer on	5	-	-	kΩ
R _O	Output impedance	The resistive load between DAC_OUT and VSS is 1.5MΩ with buffer off	-	-	15	kΩ
C _{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V _{REF+} (0xF1B) at 3.6V and V _{REF+} (0x154) at 2.4V and (0xEAC)	0.39	-	1.94	V
DAC_OUT max	High output voltage with buffer		-10.84	-	4.66	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-1.03	-	0.79	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-3.86	-	2.46	LSB
Offset	Offset error	V _{REF+} =3.6V, configuring 12-bit DAC	-2.57	-	9.49	LSB
Gain error	Gain error	Configured with 12-bit DAC	-0.0013	-	0.0045	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6. Package information

6.1. LQFP144 package diagram

Figure 17 LQFP144 Package Diagram



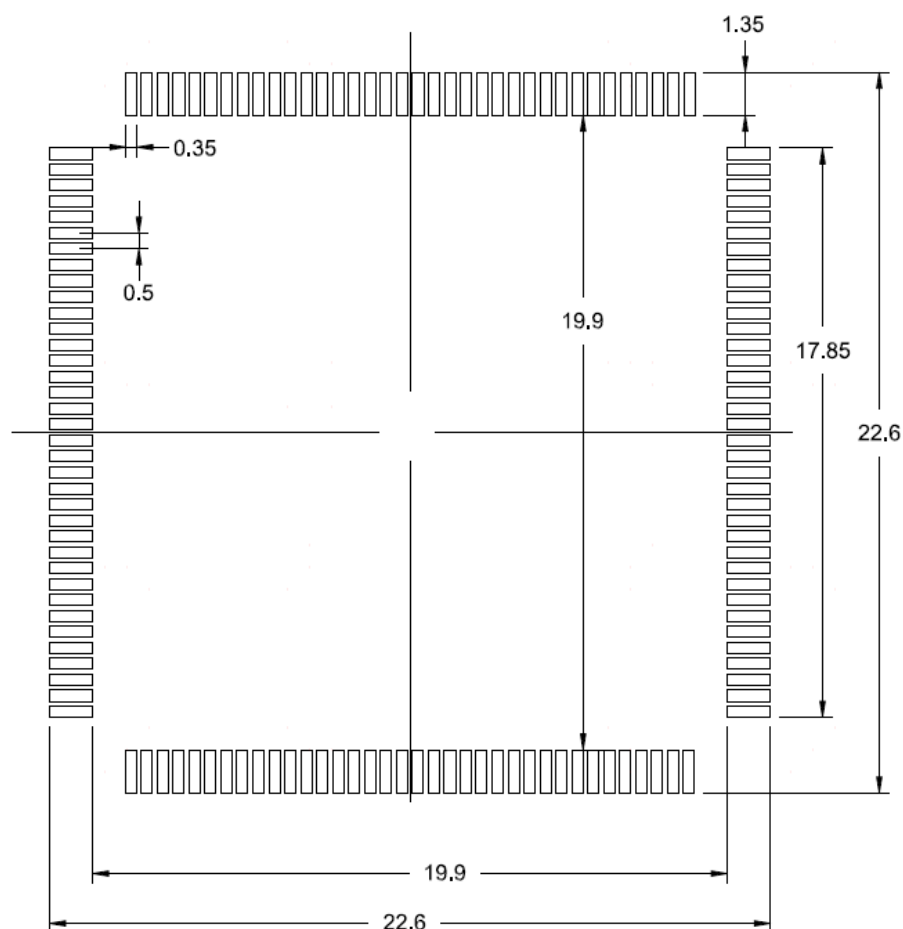
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 46 LQFP144 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	22.000±0.200	LEAD TIP TO TIP
4	D1	20.000±0.100	PKG LENGTH
5	E	22.000±0.200	LEAD TIP TO TIP
6	E1	20.000±0.100	PKG WDT
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(17.50)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

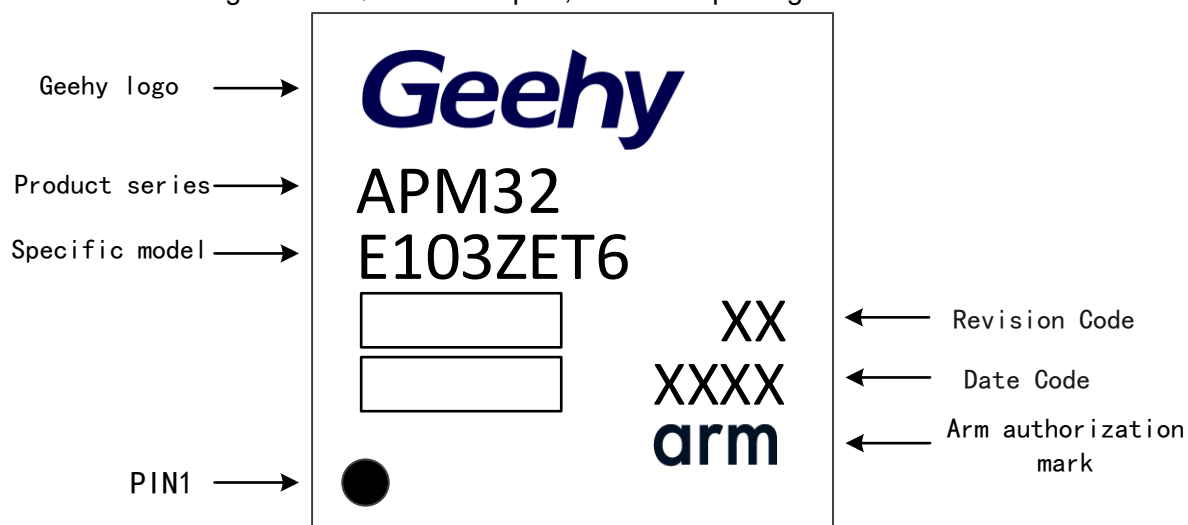
(1) Dimensions are displayed in mm

Figure 18 LQFP144-144 pins, 20×20mm recommended welding Layout



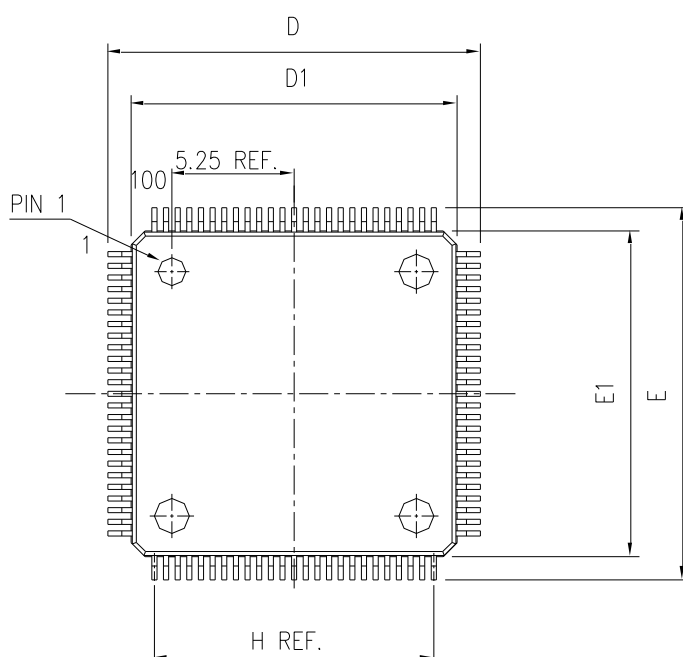
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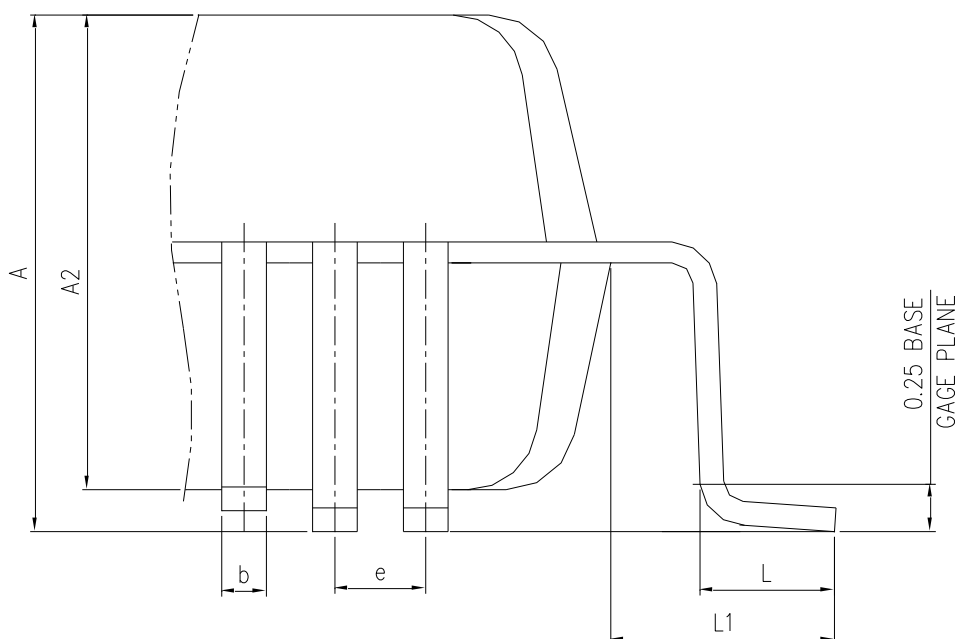
Figure 19 LQFP144-144 pins, 20×20mm package identification



6.2. LQFP100 package diagram

Figure 20 LQFP100 Package Diagram





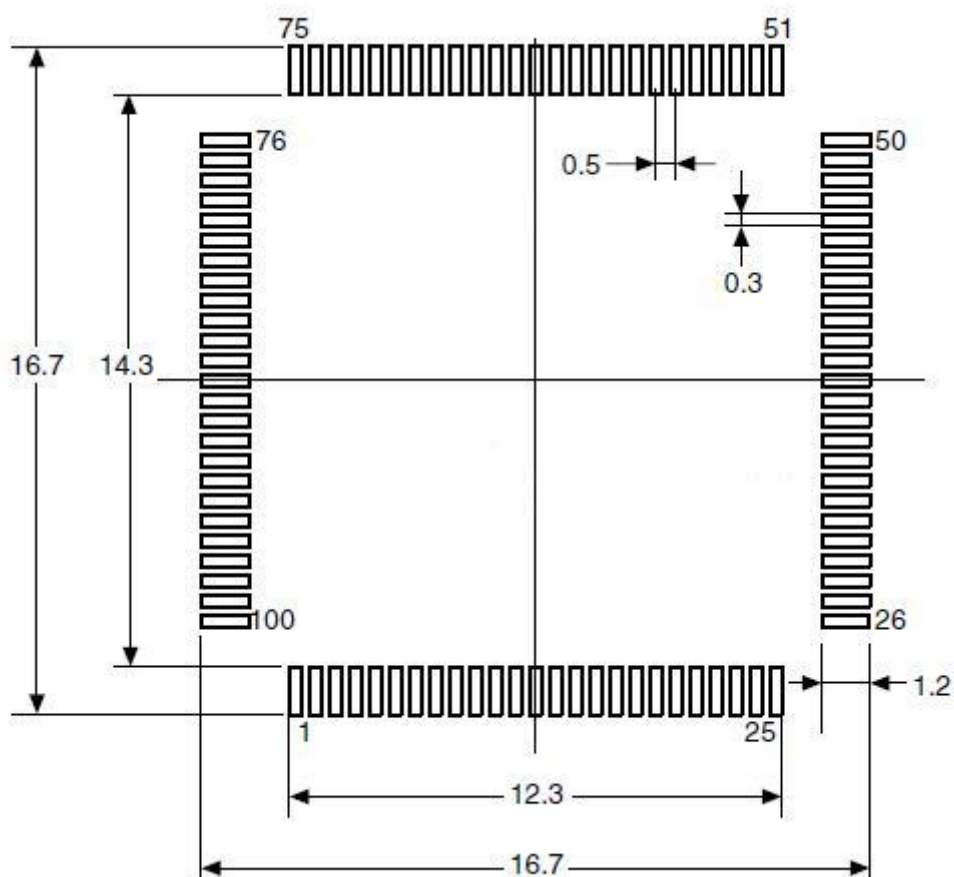
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 47 LQFP100 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(12.00)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

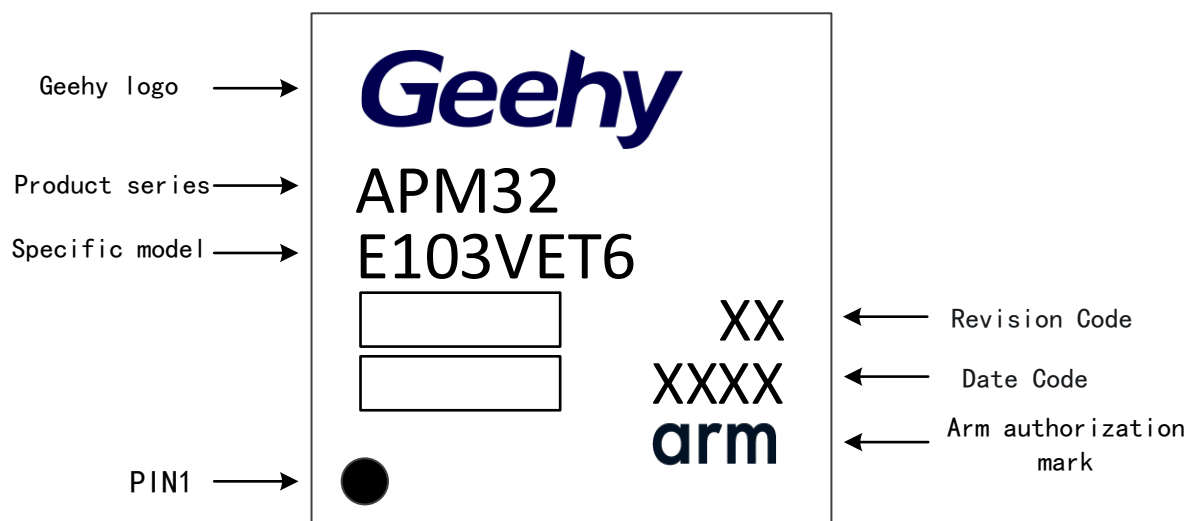
- (1) Dimensions are displayed in mm

Figure 21 LQFP100-100 pins, 14×14mm recommended welding Layout



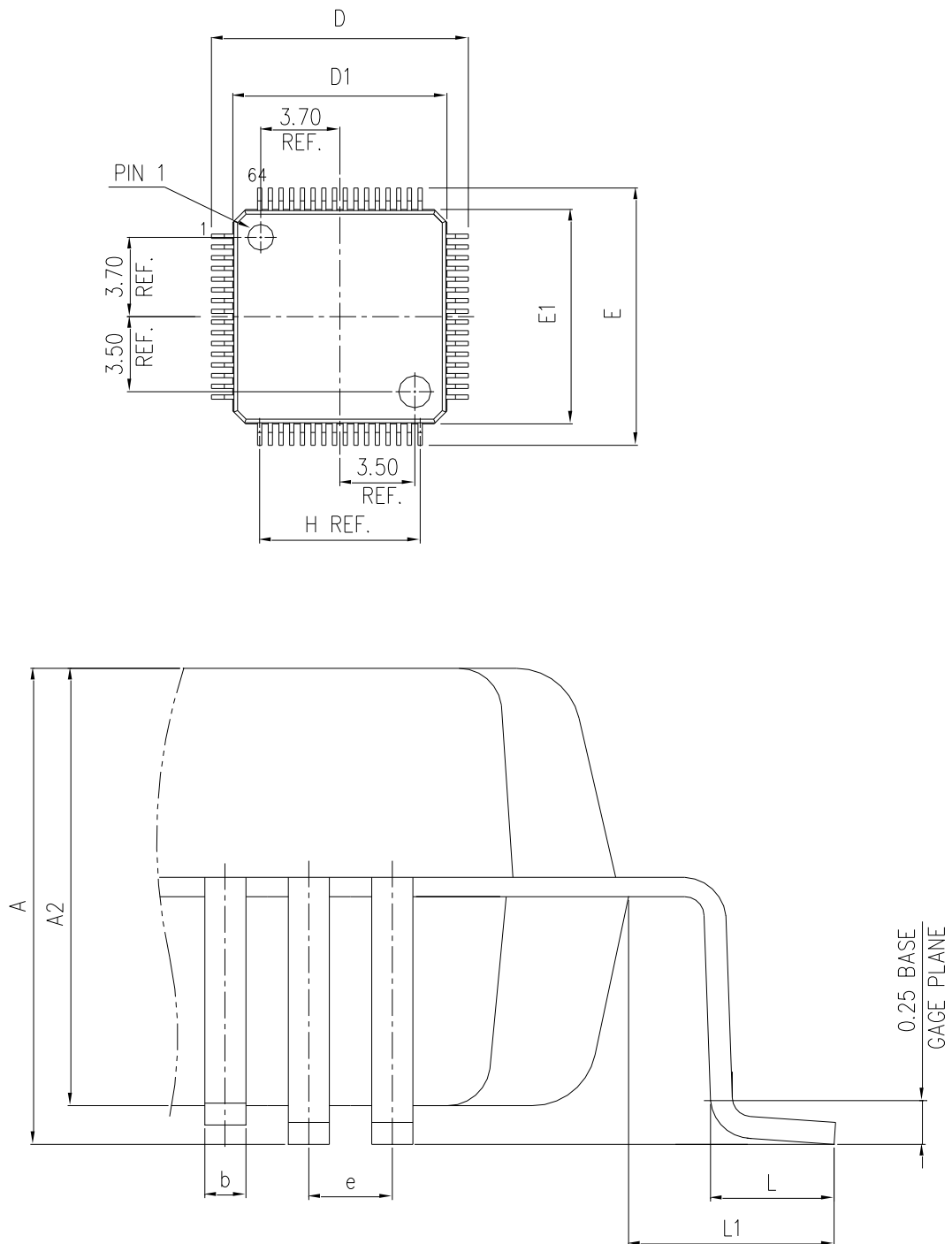
(1) Dimensions are expressed in mm

Figure 22 LQFP100-100 pins, 14×14mm package identification



6.3. LQFP64 package diagram

Figure 23 LQFP64 Package Diagram



- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 48 LQFP64 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(7.500)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

(1) Dimensions are expressed in mm

Figure 24 LQFP64-64 pins, 10×10mm recommended welding Layout

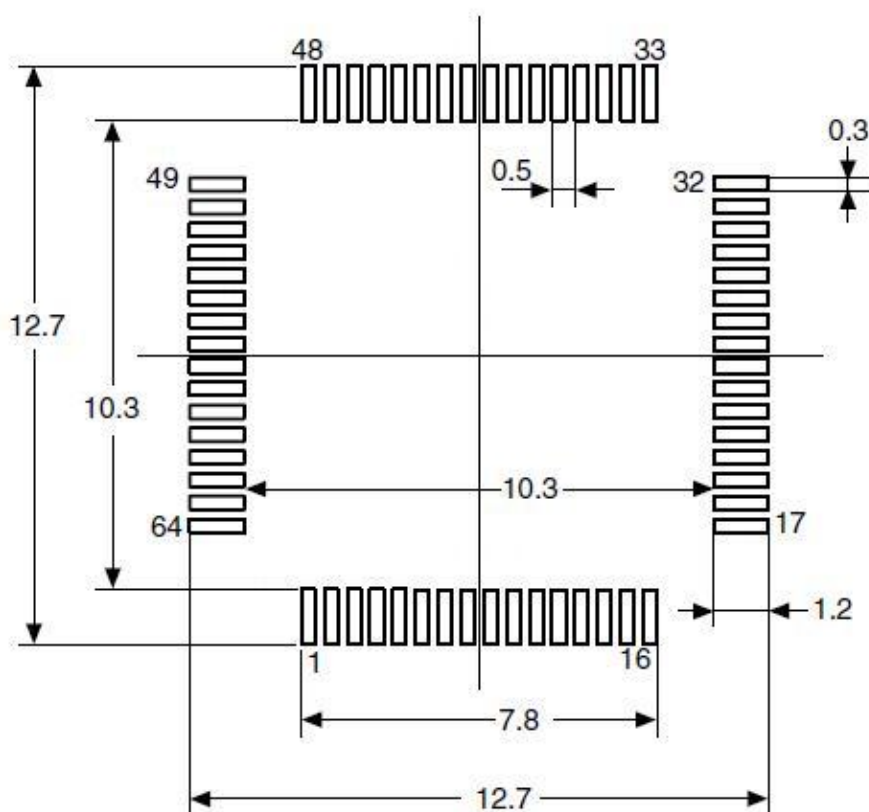
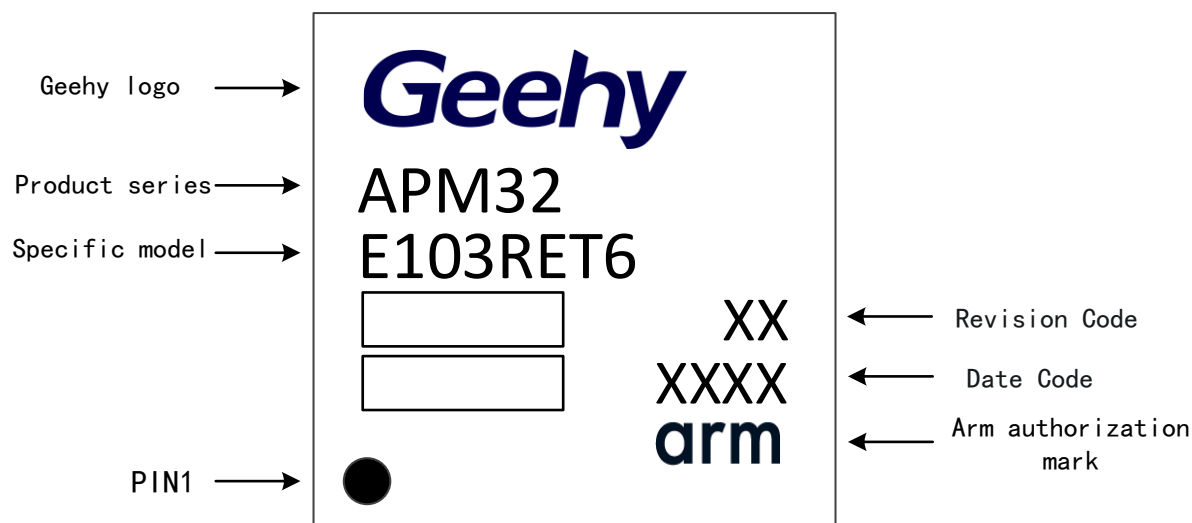
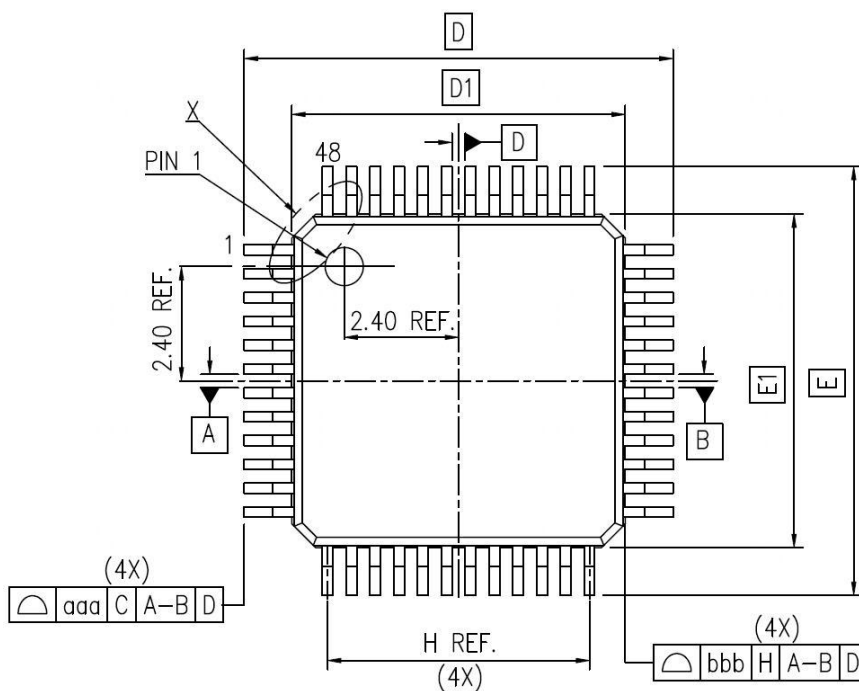


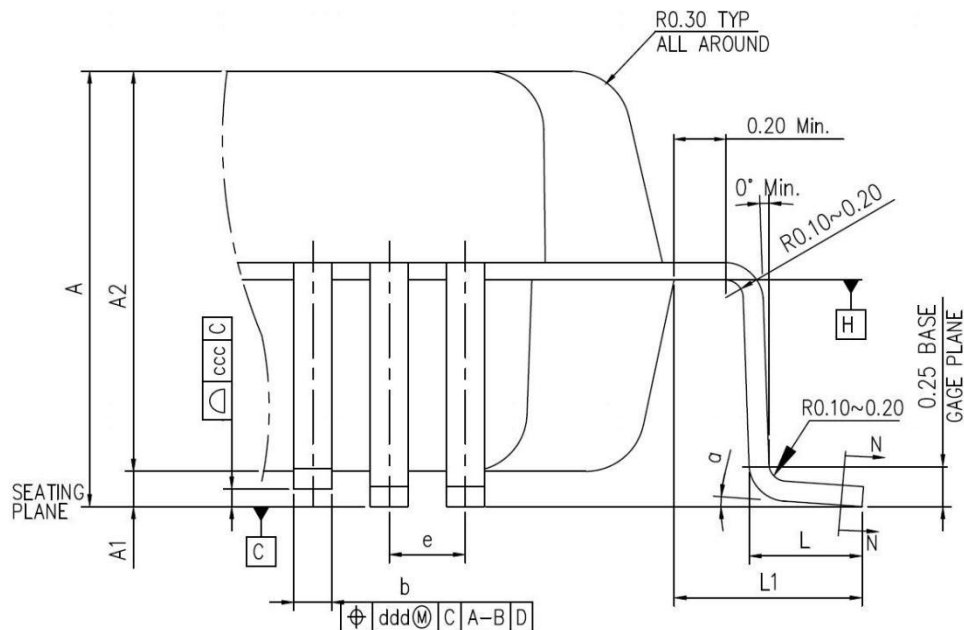
Figure 25 LQFP64-64 pins, 10×10mm package identification



6.4. LQFP48 Package Diagram

Figure 26 LQFP48 Package Diagram





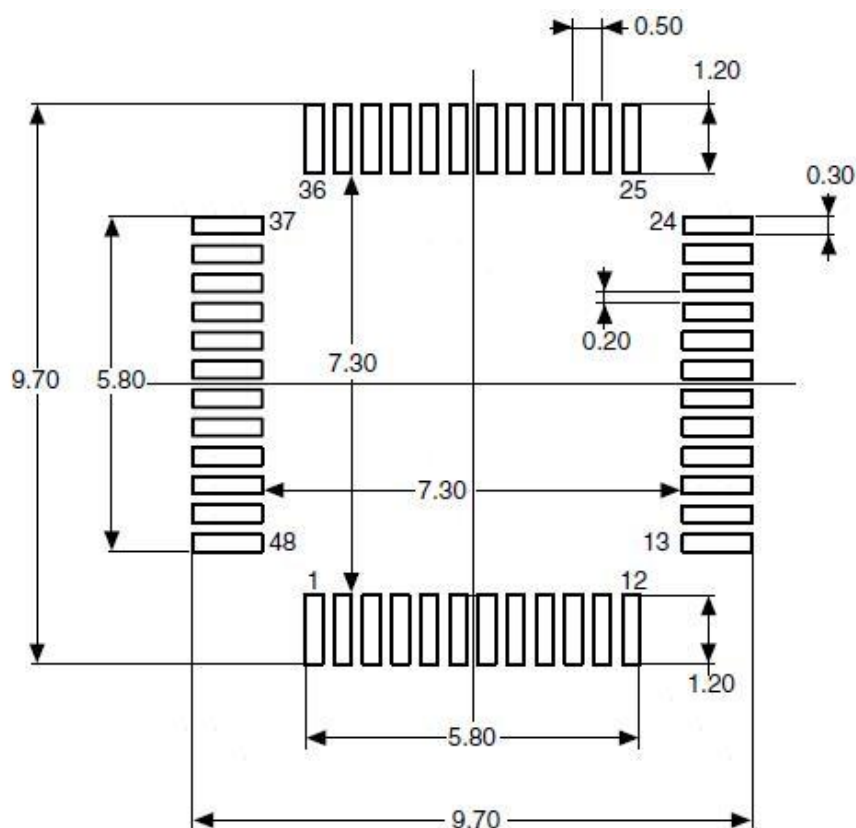
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 49 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

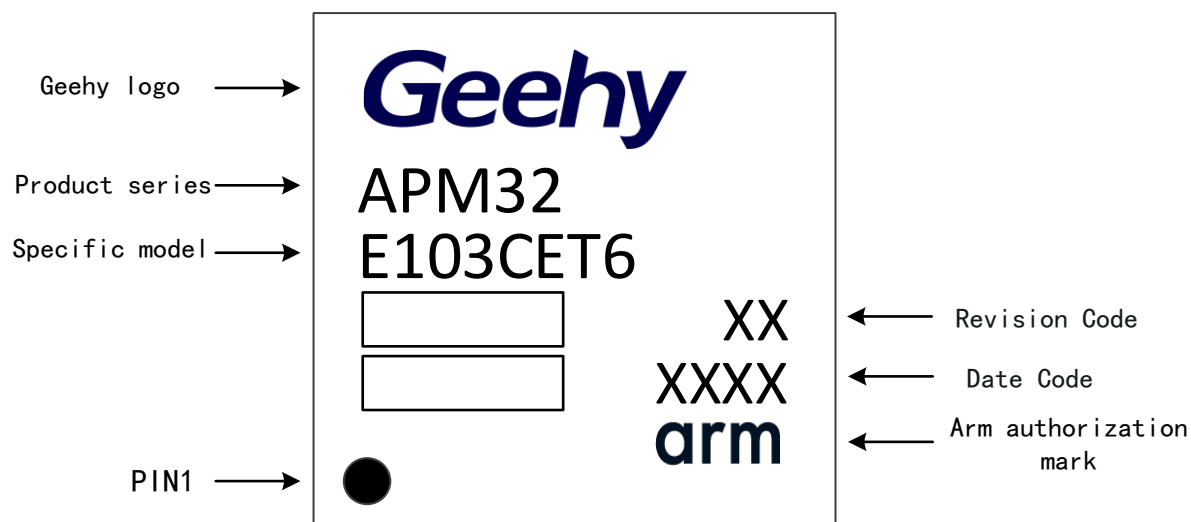
- (1) Dimensions are expressed in mm

Figure 27 LQFP48, 7×7mm recommended welding Layout



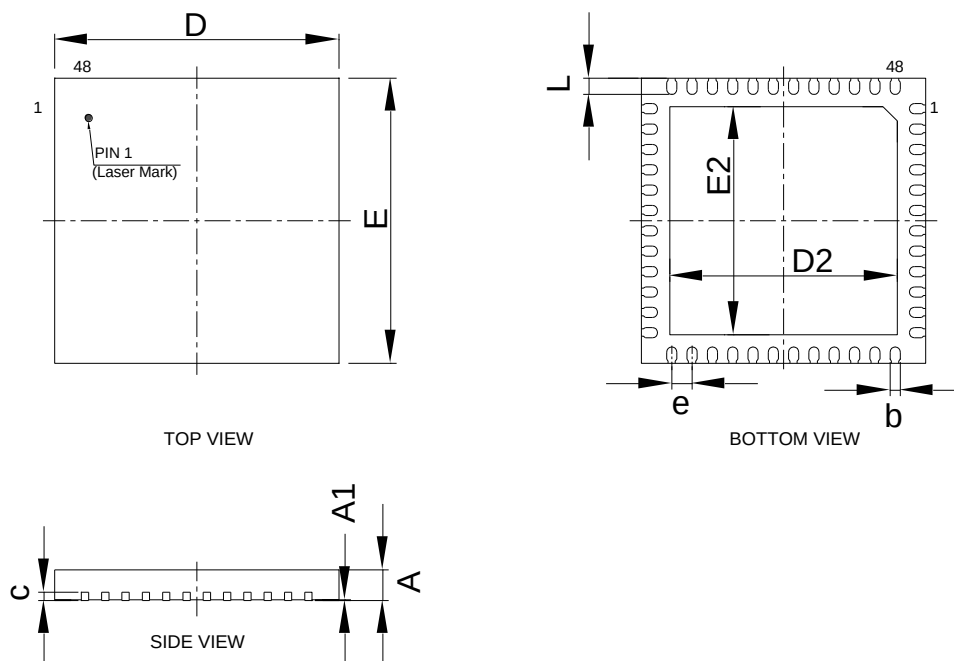
(1) Dimensions are expressed in mm

Figure 28 LQFP48-48 pins, 7×7mm identification diagram



6.5. QFN48 Package Diagram

Figure 29 QFN48 Package Diagram



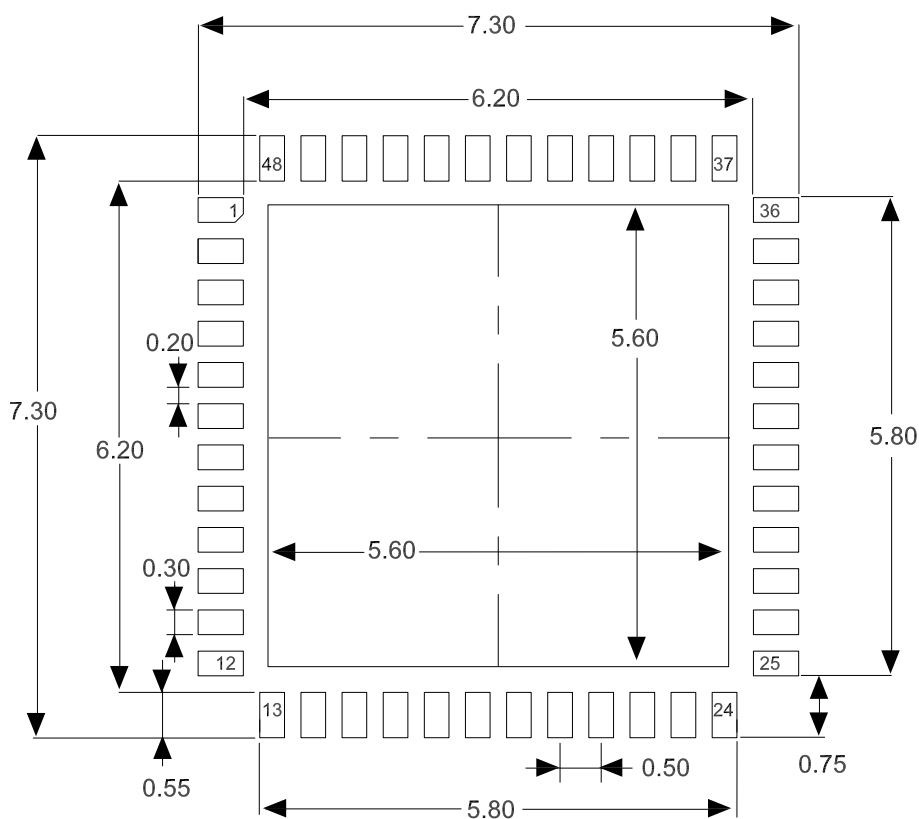
(1) The figure is not drawn to scale.

Table 50 LQFP48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
e	0.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

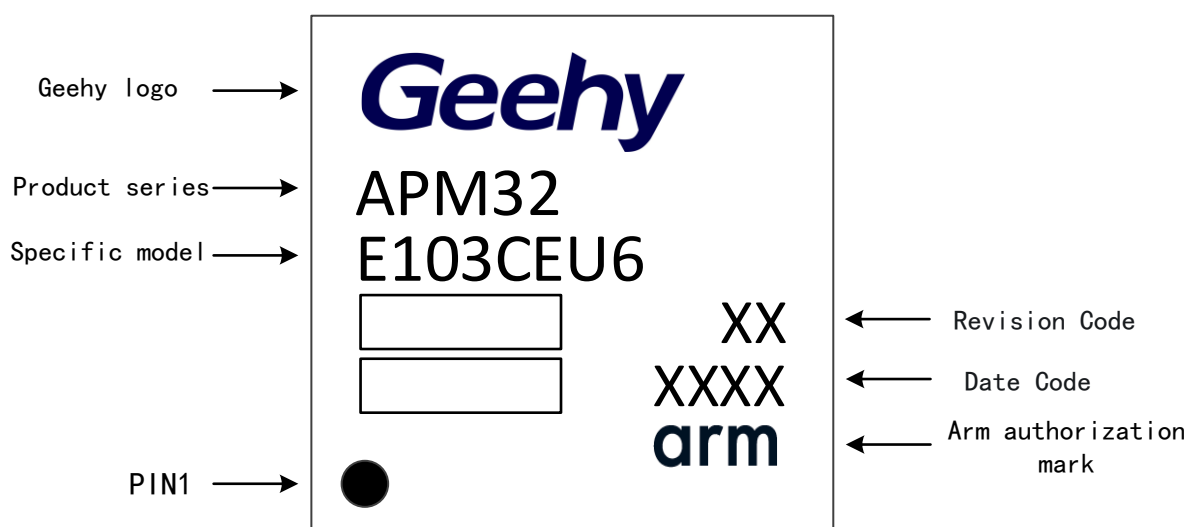
(1) Dimensions are expressed in mm

Figure 30 QFN48, 7×7mm recommended welding Layout



(1) Dimensions are expressed in mm

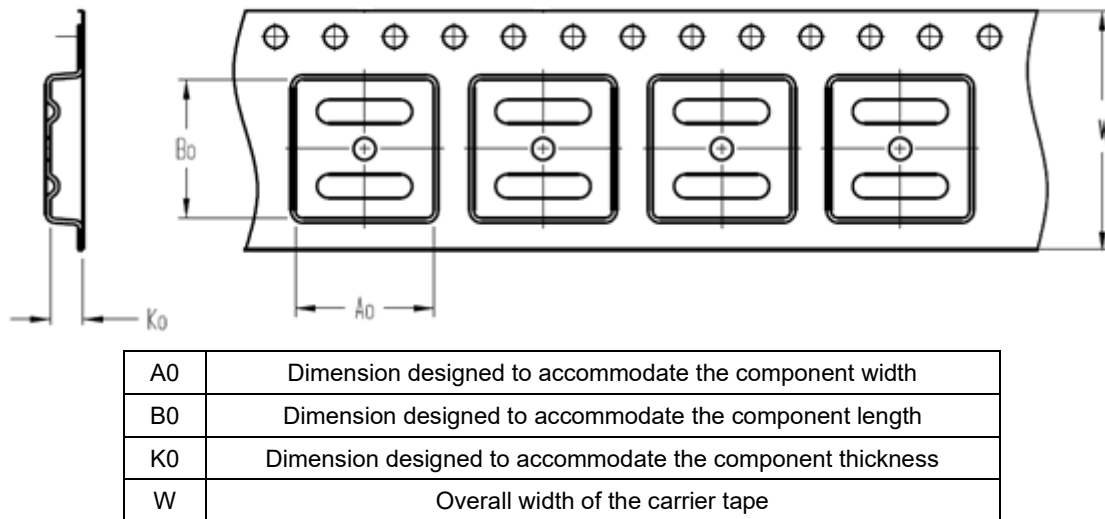
Figure 31 QFN48-48 pins, 7×7mm identification diagram



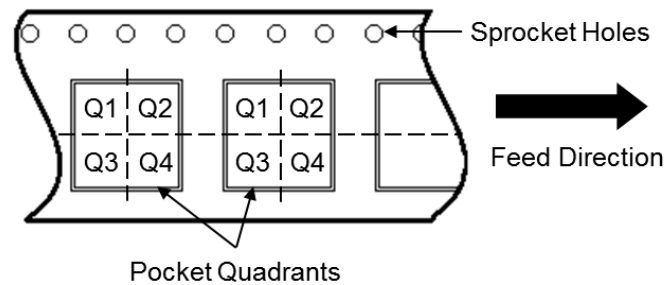
7. Packaging information

7.1. Reel packaging

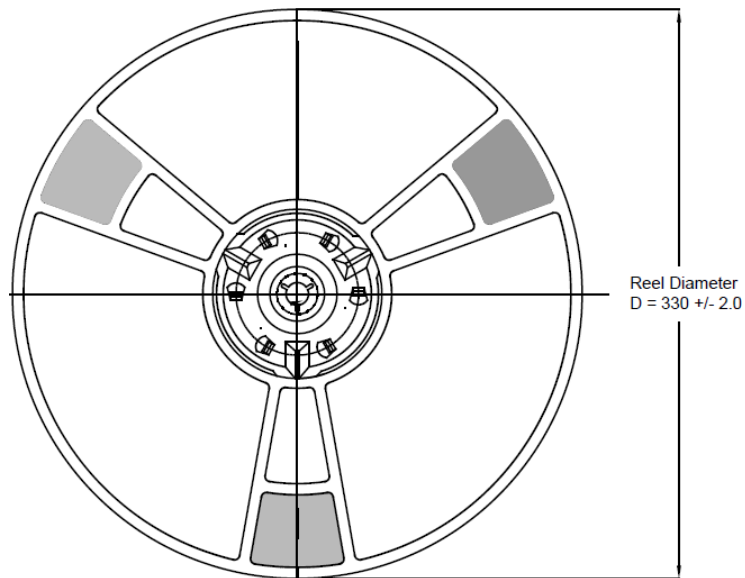
Figure 32 Specification Drawing of Reel Packaging



Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



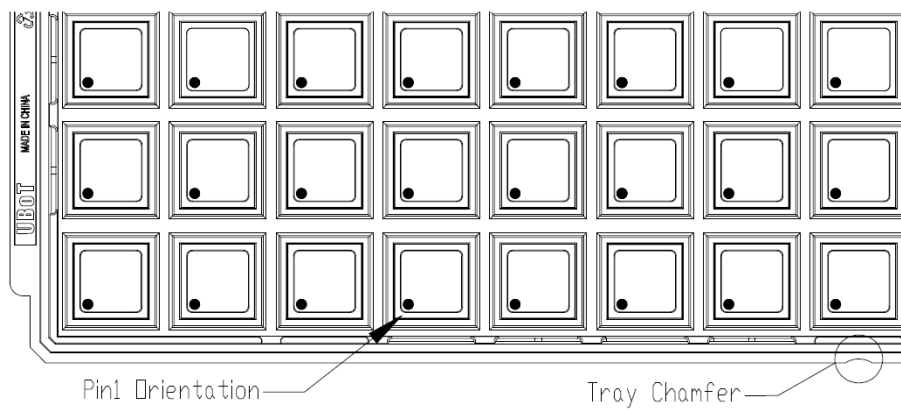
All photos are for reference only, and the appearance is subject to the product.

Table 51 Reel Packaging Parameter Specification Table

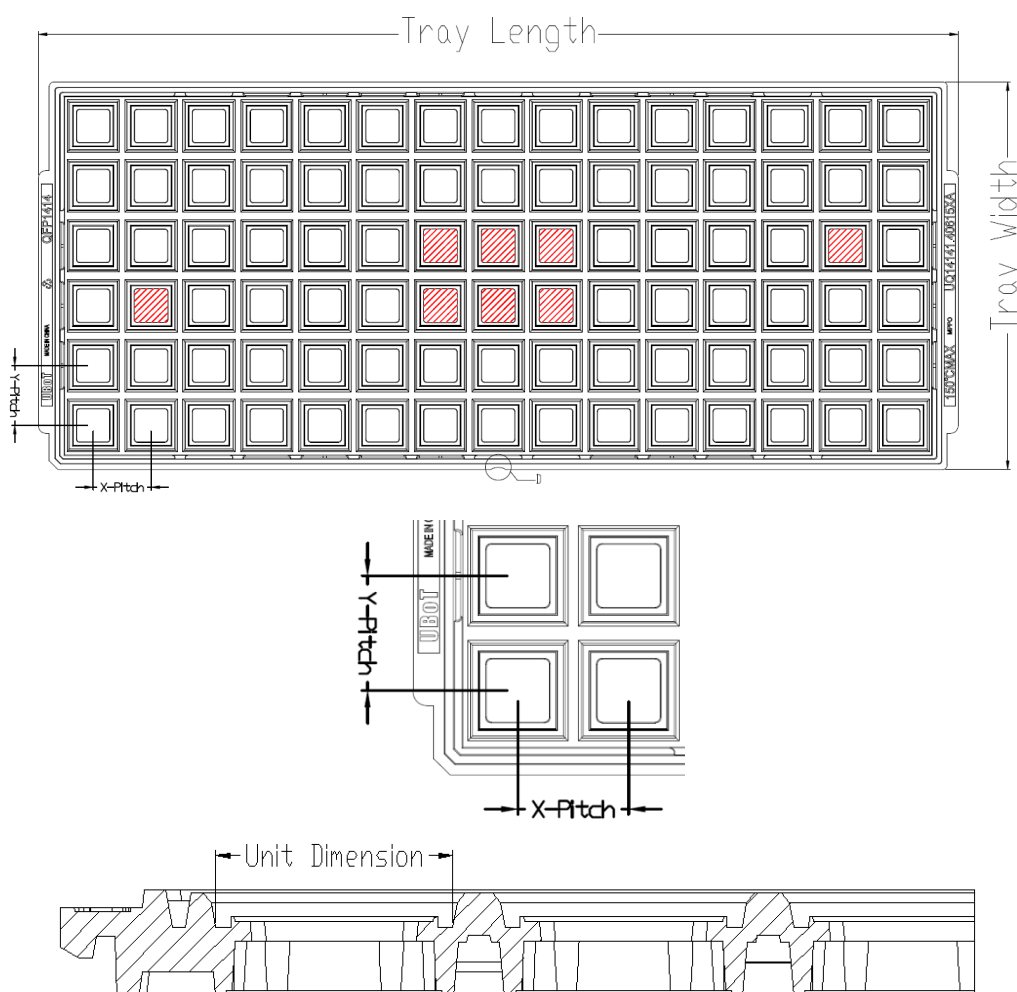
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32E103RET6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32E103RCT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32E103CET6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32E103CCT6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32E103CEU6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1
APM32E103CCU6	QFN	48	2500	330	7.4	7.4	1.4	16	Q1

7.2. Tray packaging

Figure 33 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 52 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32E103ZET6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32E103ZCT6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32E103VET6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32E103VET7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32E103VCT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32E103RET6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32E103RCT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32E103CET6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32E103CCT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32E103CEU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32E103CCU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9

8. Ordering information

Figure 34 Product Naming Rules

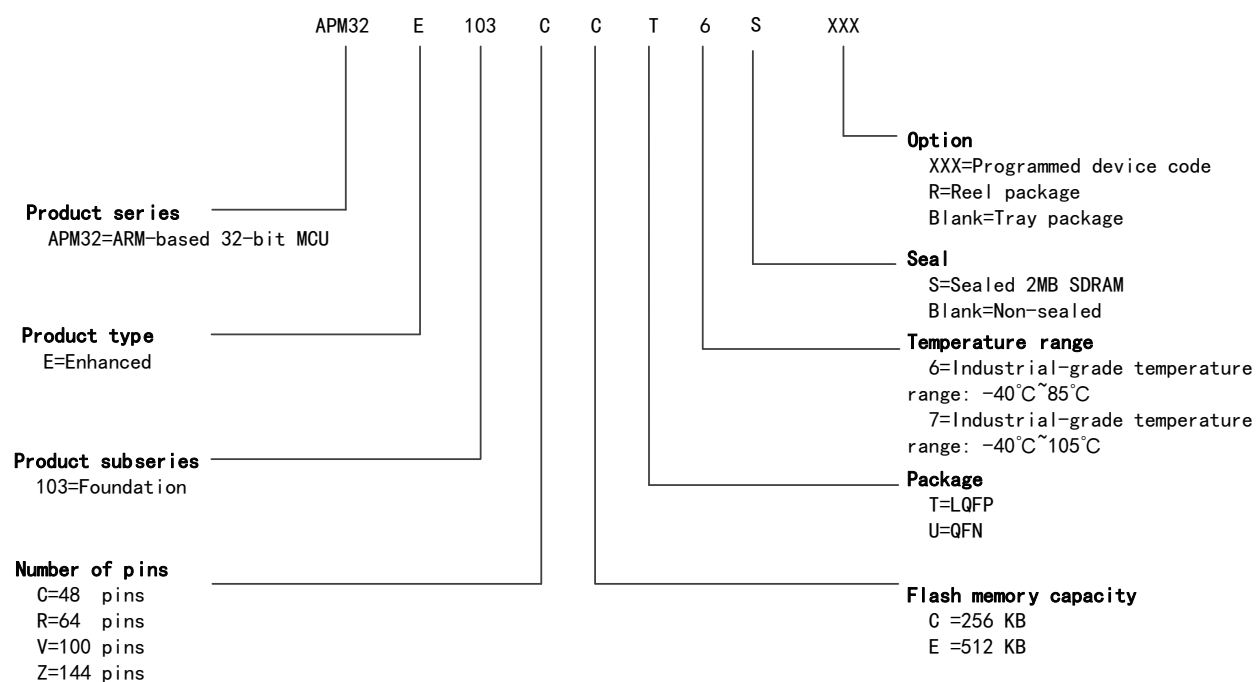


Table 53 Ordering Information Table

Order Code	Flash (KB)	SRAM (KB)	Package	SPQ	Temperature Range
APM32E103CEU6	512	128	QFN48	2600	Industrial grade -40°C~85°C
APM32E103CEU6-R	512	128	QFN48	2500	Industrial grade -40°C~85°C
APM32E103CET6	512	128	LQFP48	2500	Industrial grade -40°C~85°C
APM32E103CET6-R	512	128	LQFP48	2000	Industrial grade -40°C~85°C
APM32E103CCU6	256	64	QFN48	2600	Industrial grade -40°C~85°C
APM32E103CCU6-R	256	64	QFN48	2500	Industrial grade -40°C~85°C
APM32E103CCT6	256	64	LQFP48	2500	Industrial grade -40°C~85°C
APM32E103CCT6-R	256	64	LQFP48	2000	Industrial grade -40°C~85°C
APM32E103RET6	512	128	LQFP64	1600	Industrial grade -40°C~85°C
APM32E103RET6-R	512	128	LQFP64	1000	Industrial grade -40°C~85°C
APM32E103RCT6	256	64	LQFP64	1600	Industrial grade -40°C~85°C
APM32E103RCT6-R	256	64	LQFP64	1000	Industrial grade -40°C~85°C
APM32E103VET6	512	128	LQFP100	900	Industrial grade -40°C~85°C
APM32E103VET7	512	128	LQFP100	900	Industrial grade -40°C~105°C
APM32E103VCT6	256	64	LQFP100	900	Industrial grade -40°C~85°C
APM32E103ZET6	512	128	LQFP144	600	Industrial grade -40°C~85°C
APM32E103ZCT6	256	64	LQFP144	600	Industrial grade -40°C~85°C

Note: SPQ=Smallest Packaging Quantity

9. Commonly used function module denomination

Table 54 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10. Version history

Table 55 Document Version History

Date	Version	Change History
August 2021	1.0	New
January 2022	1.1	(1) HSICLK accuracy to 1% ~ 1% under atmospheric pressure (2) Delete the order information in the seal types of information
March 2022	1.2	Add APM32E103VET7 model
June 2022	1.3	(1) Modify Arm trademark (2) Add the statement (3) Modify product naming rules figure
October 2022	1.4	(1) Modify the pin definition for DMC_CLK (2) Modify the frequency range of LSICLK. The minimum is 30kHz and the maximum is 60kHz. (3) Modify the accuracy range of HSICLK. The minimum is -1.5% and the maximum is 1.5%. (4) Modify "CAN_RX" and "CAN_TX" to "CAN1_RX" and "CAN1_TX" in 3.2.Pin function description chapter.
August 2024	1.5	(1) Modify the USBID name in the system block diagram, address map, and pin definition (2) Modify the table of Functions and Peripherals of APM32E103xCxE Series Chips (3) Modify the address mapping figure to address mapping table (4) Add Number of erase cycles parameters in Flash Memory Characteristics (5) Add the electrical characteristics of Temperature Sensor
October, 2024	1.6	(1) Add flash storage time and erase cycle (2) Add Temperature characteristic
June, 2025	1.7	(1) Add attention points under general operating conditions (2) Add power-on/power-off characteristics
August, 2025	1.8	(1) Modify the HSICLK accuracy range

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